CAT. NO. 26-3810

TRS-80®
MODEL 100
TECHNICAL REFERENCE
MANUAL

The FCC Wants You to Know . . .

This equipment generates and uses radio frequency energy. If not installed and used properly, that is, in strict accordance with the manufacturer's instructions, it may cause interference to radio and television reception.

It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna
- Relocate the computer with respect to the receiver
- Move the computer away from the receiver
- Plug the computer into a different outlet so that computer and receiver are on different branch circuits.

If necessary, you should consult the dealer or an experienced radio/television technician for additional suggestions. You may find the following booklet prepared by the Federal Communications Commission helpful: *How to Identify and Resolve Radio-TV Interference Problems*.

This booklet is available from the US Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

Warning

This equipment has been certified to comply with the limits for a Class B computing device, pursuant to Subpart J of Part 15 of FCC Rules. Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this computer. Operation with non-certified peripherals is likely to result in interference to radio and TV reception.

Figure 6-4 LCD P.C.B. — Schematic Diagram

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240 × 64 Full Dot LCD

1/32 duty 6 bias

〈LR 202-C〉

M1 HD44102
M2 HD44102
M3 HD
M6 HD44102
M7 HD44102
M8 H
M11 HD44103
M12 HD44103

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NOTES:
1. ALL CAPACITANCE VALUES ARE INDICATED IN "μF" (P=10⁻⁶ μF).
2. ALL RESISTANCE VALUES ARE INDICATED IN "Ω" (K=10³ Ω, M=10⁶ Ω).

Figure 6-3 Main P.C.B. — Schematic Diagram

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Section 1. System Overview

Radio Shack's TRS-80 Model 100 is a portable computer equipped with built-in software to perform a variety of useful tasks such as text preparation, schedule and address organizing, and telecommunications.

Additionally, Model 100 has the following standard features:

- Enhanced version of Microsoft BASIC

- Full-size typewriter style keyboard

- LCD with seven lines by 40 columns

- Built-in modem

- Built-in cassette interface

- Built-in bar code reader interface

- Parallel printer interface

Other features available are: real time clock and calendar, upper- and lowercase characters, and RAM internally expandable to 32K bytes.

Specifications

Main Components

Keyboard
71 keys (9 x 8 matrix)

Alphabet keys	27
Number keys	10
Picture-control keys	7
Function keys	8
Special symbol keys	8
Mode keys	5
Other special-use keys	6

Specifications Cont'd

LCD display
Display panel	240 x 64 Full-Dot matrix
	1/32 duty
	1/6.66 bias
Dot pitch	0.8 x 0.8 mm
Dot size	0.73 x 0.73 mm
Effective display area	191.2 x 50.4 mm

Operation batteries
Batteries	Four AA alkaline-manganese batteries
Operation time	5 days (at 4 hours/day)
	20 days (at 1 hour/day)
	Note: I/O is disconnected.

Memory protection battery (on Main PCB)
Battery	Rechargeable
Protection time	About 40 days (8 KB)
	About 10 days (32 KB)
Recharge method	Trickle charge by AC adaptor, or operation batteries

LSIs
CPU	80C85
	Code and pin compatible with 8085
ROM	Max. 64 KB (2 banks of 32 KB)
	Standard 32 KB
	Option 32 KB
RAM	Max. 32 KB
	Standard 8 KB RAM pack
	Incremental 8 KB RAM pack on PCB

Clock/Calendar
	μPD1990AC
	No leap year/no February 29

I/O Interface

RS-232C (conforms to EIA Standard)
Signal	TXR (Transmit Data)
	RXR (Receive Data)
	RTS (Request to Send)
	CTS (Clear to Send)
	DSR (Data Set Ready)
	DTR (Data Terminal Ready)

Communications protocol	
Word length	6, 7, or 8 bits
Parity	NON, EVEN, or ODD
Stop Bit length	1 or 2 bits
Baud rate	75, 110, 300, 600, 1200, 2400,4800, 9600, 19200 BPS

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Specifications Cont'd

Max. transmission distance	5m
Driver max. voltage output	± 5V
Driver min. voltage output	± 3.5V
Receiver max. voltage input	± 18V
Receiver min. voltage input	± 3V

Modem/coupler (conforms to BEL103 standards)

Baud rate	300 BPS
Programmable items:	
Data length	6, 7, or 8 bits
Parity	NON, EVEN, or ODD
Stop bit	1 or 2 bits
Full duplex	Answer/call switchable mode
Other functions	Hang-up and auto-dialer

Audio cassette interface

Data rate	1500 BPS
	(MARK: 2400 Hz, SPACE: 1200 Hz)

Printer interface (conforms to Centronics interface standards)

Handshake signal	$\overline{STROBE}$, BUSY, $\overline{BUSY}$

Controls and Functions

Power switch. Move this switch toward the front to turn the power ON. To conserve the batteries, Model 100 automatically turns the power off if the unit is not used within 10 minutes. When an automatic power-off occurs, the switch remains in the ON position even though the power is off. To turn the power on, move the switch to the OFF position, then back to ON.

ANS/ORIG selector. Selects the modem answer mode or call mode. If you are originating a phone call to another computer, set the switch to ORIG. If another computer is calling your Model 100, set to ANS.

DIR/ACP selector. This switch allows you to select either direct connection or acoustic coupler modem connection. If you are communicating with another computer by telephone via the built-in Direct Connect Modem, set the switch to the DIR position. If you are using the optional/extra Model 100 Acoustic Coupler (*Radio Shack Catalog Number 26-3805*), set the selector to the ACP position.

Memory power switch. This switch prevents over discharge of the Ni-Cad battery for RAM back-up. Model 100 will not operate regardless of the setting of the power switch unless this switch is on. Set the switch to OFF if the Model 100 is not to be used for a long time. Note that the RAM will not be backed up when this switch is set to OFF.

RESET switch. If the Model 100 "locks up" (i.e., the display "freezes" and all keys appear inoperative), press this button to return to the Main Menu (start-up) screen. It's highly unlikely that the Model 100 will lock-up when you are using the built-in application programs. However, this situation may occur with customized programs.

Display adjustment dial. This control adjusts the contrast of the LCD display relative to the viewing angle.

Special Function — Automatic Power OFF.

When there is no program operation (awaiting command) for ten minutes, the power is automatically cut off.

To start again, the power switch must be turned OFF and then ON, thus releasing the automatic power OFF condition. (The display will be the same as before the power was turned off.)

Connectors

RS-232C	25 pins (DB-25S)
Printer	26 pins (FRC2-C26-L13-ON)
Modem	8 pins (TCS-4490)
Cassette	8 pins (TCS-4480)
Bar code reader	9 pins (A-7224)
System Bus	40 pins (IC Socket)
AC adapter	5.5 (Center Minus)

Section 2. Disassembly/Reassembly

This section describes the procedures for disassembling and reassembling the Model 100 Portable Computer.

To disassemble the computer:

Case

1. Disconnect all cables from the unit (printer cables, cassette cables, etc.).

2. Turn the Computer over and place it on a piece of cloth or another soft material to prevent scratching the Display. Remove the four screws Ⓐ near the corners to separate the lower case (black area) from the upper case.

3. Turn the Computer over again and remove the upper case, opening it to the right side. Note that the upper and lower case are also held by snaps. You'll need to pull the upper case firmly, but gently. (The LCD, Keyboard, and Buzzer are connected to the CPU Board in the lower case.)

4. Remove the LCD, the Keyboard, and the Buzzer connectors from the CPU Board.
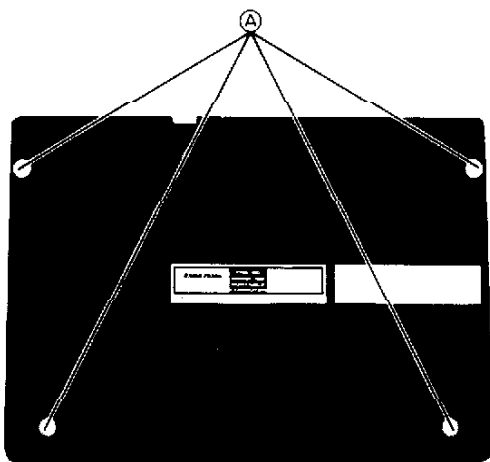
Figure 2-1. Bottom View
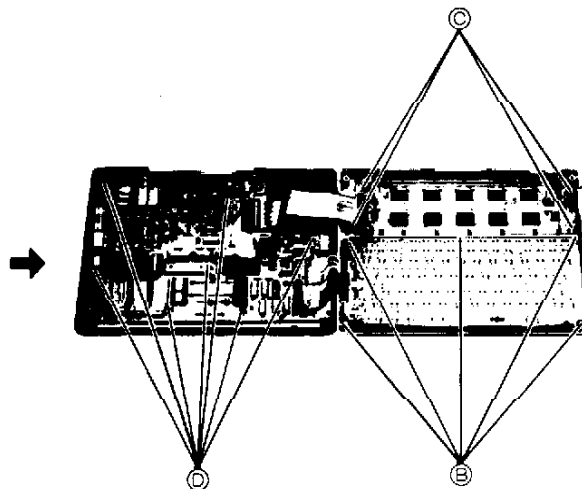
Figure 2-2. Interior View

Keyboard PCB

1. Remove the five screws ⑧ from the Keyboard PCB on the upper case and then remove the Board.

2. Remove the Keyboard PCB supports.

LCD Board

Remove the four screws ⓒ from each corner of the LCD and then remove the Board.

CPU Board

1. Remove the seven screws ⓓ holding the CPU board to the lower case.

2. Remove the CPU Board by lifting it upward. Be especially careful when removing the RESET Switch and the battery contact spring.

To reassemble:

CPU Board

1. Align the screw positions of the lower case with the CPU Board. Then insert the CPU Board, starting at the rear. Be sure that the RESET Switch fits properly in its notch.

2. Secure the battery contact spring.

3. Secure the CPU Board to the lower case with the seven M3 x 8 screws.

LCD PCB

1. Secure the LCD Board to the upper case with the four M3 x 3 screws.

2. Insert the Buzzer connector in the LCD Board to the CPU Board.

Keyboard PCB

1. Align the two Keyboard supports with the holes in the Keyboard PCB and attach so that they fit on the PCB's longer edges.

2. Align the Keyboard supports and holes with the upper case screws.

3. Attach the Keyboard supports and the Keyboard PCB to the upper case using the five M3 x 8 screws.

Case

1. Double-check to be sure all wires are connected correctly and all boards are properly fastened.

2. Place the upper and lower cases side by side with the upper case next to the right side of the lower case. (Be careful not to scratch the Display.)

3. Attach the LCD and Keyboard connectors to the CPU Board in the lower case.

4. Carefully swing the upper case over the lower case. Avoid pulling on the connecting cables.

5. Align the upper and lower cases so that the tabs fit well.

6. Hold both cases together, turn the unit over and secure with the four M3 x 8 screws.

Section 3. Theory of Operation

TRS-80 Model 100 has three principal LSIs:

- 80C85 Central Processing Unit (CPU) that controls all functions

- 81C55 Parallel Input/Output (PIO) interface controller that controls the parallel printer, keyboard, buzzer, clock, and LCD

- IM6402 Universal Asynchronous Receiver Transmitter (UART) that controls the serial interface (RS-232C or modem)

The block diagram shows the various internal components and connections of Model 100.
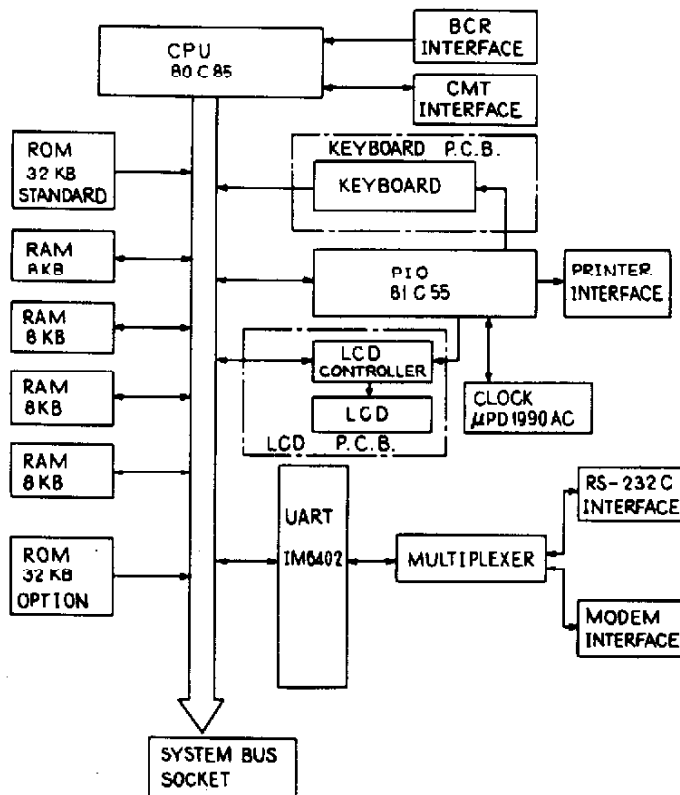
Figure 3-1. Block Diagram

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The input/output for a cassette recorder and the input of the BCR are controlled by CPU directly through its SOD, SID, and RST 5.5 terminals.

ROM and RAMs are connected to the System Bus. ROM is available only for alternative selection of standard or optional.

Technical Description

The technical description of the Model 100 is divided into 17 sections.

1. Processor
2. Memory
3. Address Decoding and Bank Selection
4. Memory Map
5. I/O Map and I/O Port Description
6. Keyboard
7. Cassette Interface
8. Printer Interface
9. Bar Code Reader Interface
10. Buzzer Control Circuit
11. System Bus
12. LCD Interface
13. Clock Circuit
14. Serial Interface
15. Liquid Crystal Display
16. Power Supply and Auto Power OFF Circuit
17. Reset Circuit

This breakdown, which corresponds with the partitioning of the schematic diagrams, will allow easy explanation and referencing.

Processor

Model 100 uses a MSM80C85ARS (80C85) CPU chip, a complete 8-bit parallel Central Processing Unit. With an instruction set that is 100 percent software-compatible with the 8080A microprocessor, 80C85 represents an improvement over 8080A's performance with a higher system speed.

80C85 uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus.

The data and address buses are separated by M1 (TC40H373P: Octal "D" type latch). The performance of the bus line is increase by M2 (TC40H245P: Octal bi-directional bus buffer) and M21 (TC40H244P: Octal buffer/driver).

Memory

Model 100's memory consists of a 32K ROM and up to 32K of RAM (standard RAM is 8K). Three RAM increments — 8K each — are possible. Also, an additional (optional) 32K BANK ROM can be installed.
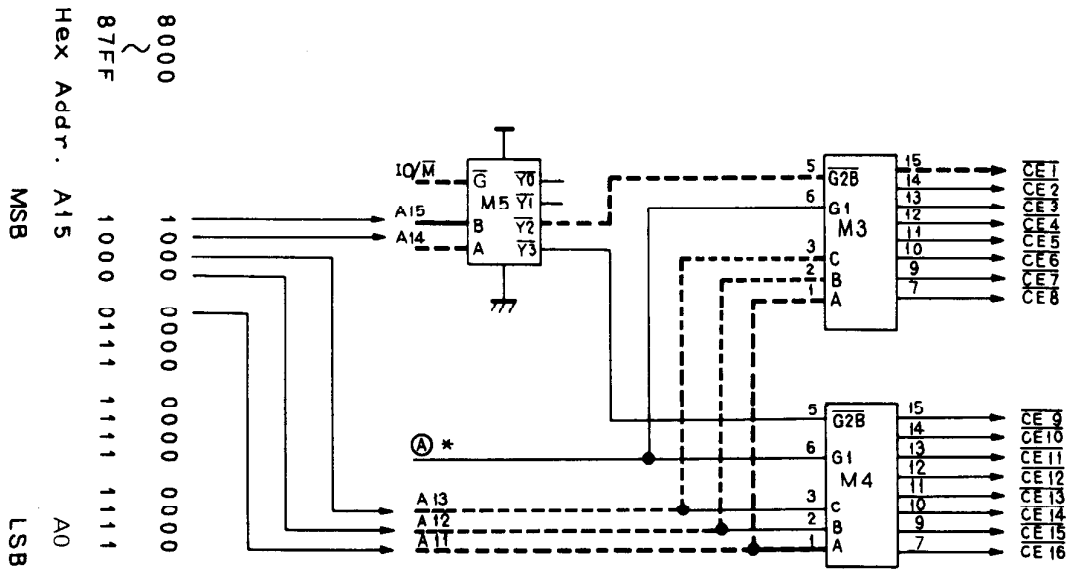
Address decoding for RAM chip 1
(8000H to 87FFH)
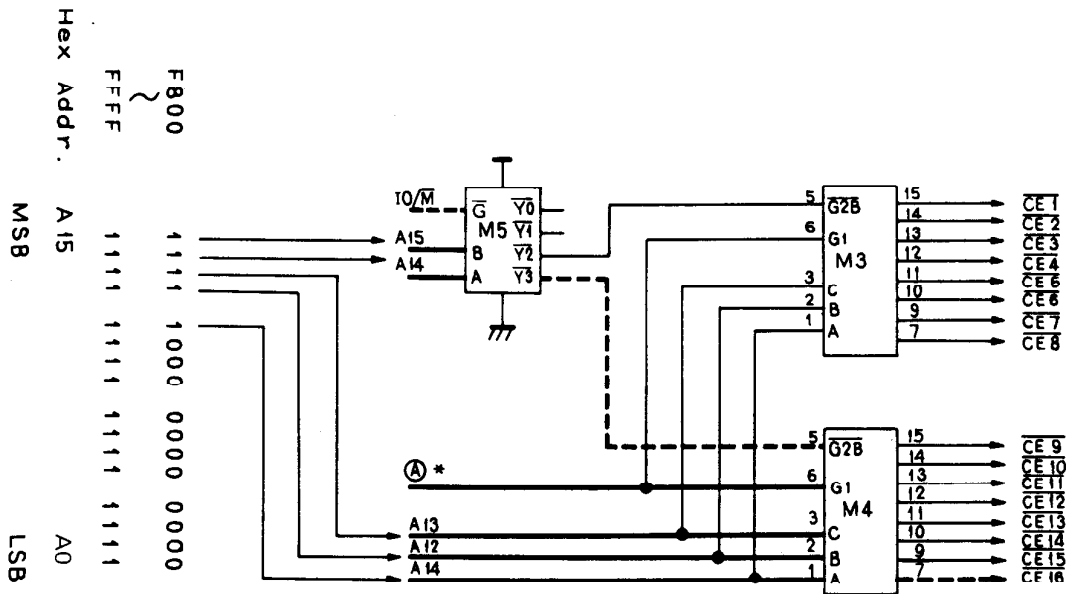
Address decoding for RAM chip 16
(F800H to FFFFH)

Figure 3-3. Address Decoding for RAM Chip

ROM Chip Selection. ROMs (both standard and optional) used in the Model 100 are the 32K 1-chip type. As shown on the Memory Map, the address space is positioned from 0000H to FFFFH.

Chip-select signals are generated by A15 and $\overline{\text{STROM}}$.

Random Access Memory (RAM)

Model 100 has a RAM pack consisting of four 2K RAMs (each 2048 x 8 bits) mounted on the ceramic motherboard for a total of 8K (8192 x 8 bit).

The standard RAM pack for the Model 100 is the M9. Memory capacity can be increased up to 32K, however, by installing M6, M7, and M8.

The internal wiring diagram of the RAM pack is shown in Figure 3-2.
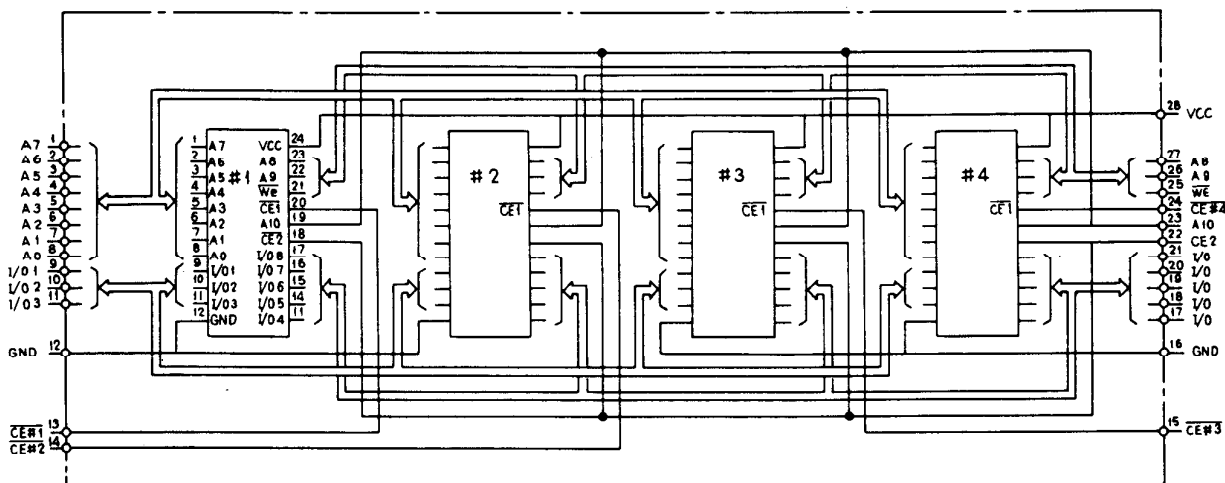
Figure 3-2. Internal Wiring Diagram of RAM Pack

Read Only Memory (ROM)

Model 100 uses a synchronous 32K ROM (256K bits). Operated by a single 5-volt power supply, the access time is 600nsec (max). The ALE (Address Latch Enable) is used as the synchronous signal with the CPU. The BASIC program is stored in the standard ROM. The BIOS program is stored in the standard ROM for operation of the LCD, printer, etc.

An optional ROM can be installed in the special IC socket by removing the ROM cover on the bottom case of the Model 100. A variety of application programs can be entered in the optional ROM.

Address Decoding and Bank Selections

RAM Chip Selection. Although four 8K RAM packs are attached to the Model 100, 16 chip-select signals are necessary since 16 x 2K RAMs are actually used.

Moreover, because the RAM area is addressed from 8000H to FFFFH (see Figure 3-3), the control signal is formed by IO/$\overline{M}$, A15 and A14 as shown in Figure 3-3. The 16 chip-select signals are formed by A13, A12, and A11.

M5 (TC40H139: dual 2 to 4-line decoder/demultiplexer) generates the control signal. M3 and M4 (TC40H138: 3 to 8-line decoder/demultiplexer) generate the 16 chip-select signals.

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As shown in Figure 3-4, AD0 is latched at M14 (TC40H175 quad ''D'' type F/F) by signals $\overline{WR}$ and $\overline{Y6}$, then $\overline{STROM}$ is generated. (Refer to the I/O port description.)

The chip-select signal of each ROM is generated by $IO/\overline{M}$ signal at M5 (TC40H139). The standard ROM is selected by the L $\overline{STROM}$ signal and the optional ROM by the H $\overline{STROM}$ signal.
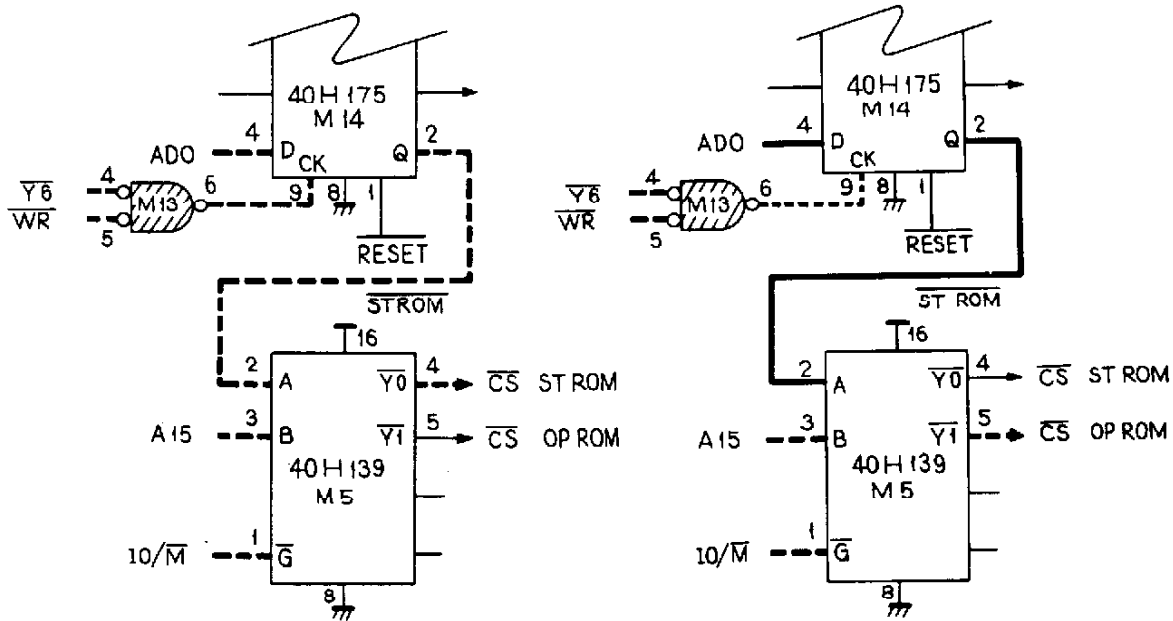
Standard ROM chip selection   Optional ROM chip selection

——————— Active line with high-level

— — — — — Active line with low-level

Figure 3-4. Standard and Optional ROM Selections

Model 100 Memory Map
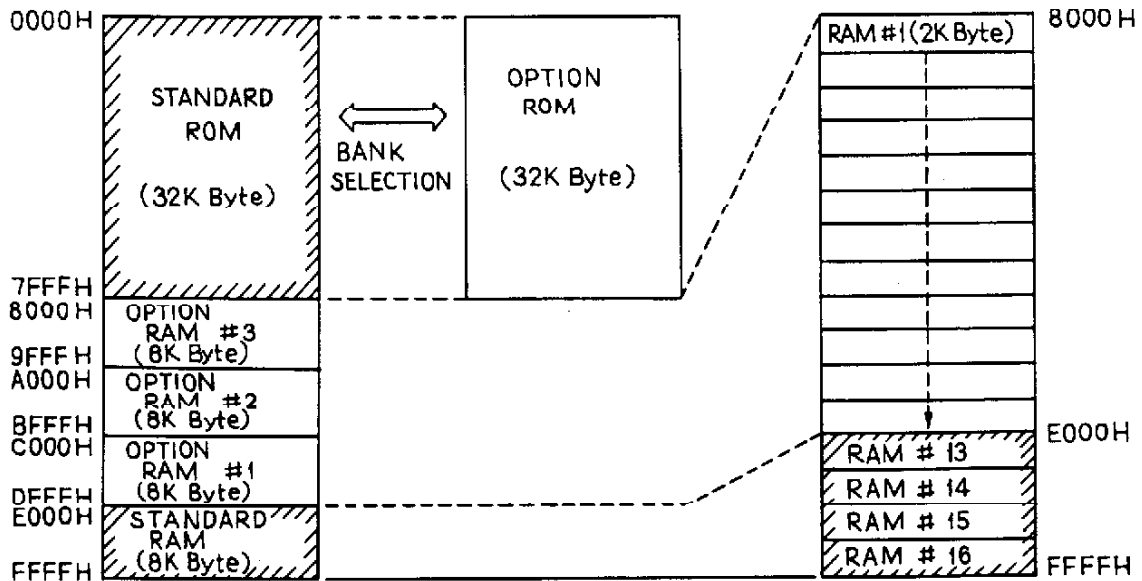
Addressing of additional RAMs start from higher address.

Figure 3-5. Memory Map

I/O Map and I/O Port Description

As shown in Figure 3-6, the I/O address decoder circuit, consisting of M-16 (40H138), decodes address signals A12 to A15 and generates the I/O control signals $\overline{Y0}$ to $\overline{Y6}$ and Y7.
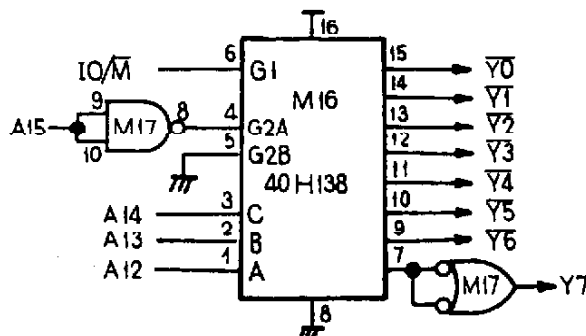
Figure 3-6. I/O Address Decoder Circuit

Because the LCD driver-select signal Y7 is active H, the output of M16 (40H138) is inverted by M17 (40H000). Table 3-1 shows how select signals ($\overline{Y0}$ to $\overline{Y6}$ and Y7) for the I/O device and address are used.

Address	Signal	Active Level	Application
70H-7FH	—	—	Free area for optional RAM unit and other select signals of circuits made by user.
80H-8FH	$\overline{Y0}$	L	Device-select signal for optional I/O controller unit.
90H-9FH	$\overline{Y1}$	L	Device-select signal for optional answering telephone unit.
A0H-AFH	$\overline{Y2}$	L	Bit 0: ON/OFF of relay for signal selection of telephone unit. Bit 1: Generates ENABLE signal of LSI (MC14412) for MODEM.
B0H-BFH	$\overline{Y3}$	L	PIO (81C55) chip-select signal.
C0H-CFH	$\overline{Y4}$	L	ENABLE signal for data input/output port of UART (IM6402).
D0H-DFH	$\overline{Y5}$	L	ENABLE signal to set various modes and read port of UART.
E0H-EFH	$\overline{Y6}$	L	ENABLE signal for STROM and REMOTE, and input data from keyboard. Also, strobe signal for printer and clock.
F0H-FFH	Y7	H	ENABLE signal for LCD driver LSI (HD14403).

Table 3-1. I/O Map

Table 3-2 below shows the I/O address of each port of PIO (81C55)

Address	Port or Register
B0H or B8H	Command/status (Internal)
B1H or B9H	Port A
B2H or BAH	Port B
B3H or BBH	Port C
B4H or BCH	Timer register lower byte
B5H or BDH	Timer register upper byte
B6H, B7H, B8H, and B9H	Not used

Table 3-2. I/O Address of Each Port

Keyboard Control Circuit

Key strobe signals are emitted from PB0 and PA0 - PA7 of 81C55, and the return signals from the keyboard pass through the octal bus buffer IC (40H244) to the CPU. Data input port I/O address at this time is E0H - EFH. The keyboard control circuitry is shown in Figure 3-7. This figure shows the circuit condition when (T) is pressed.
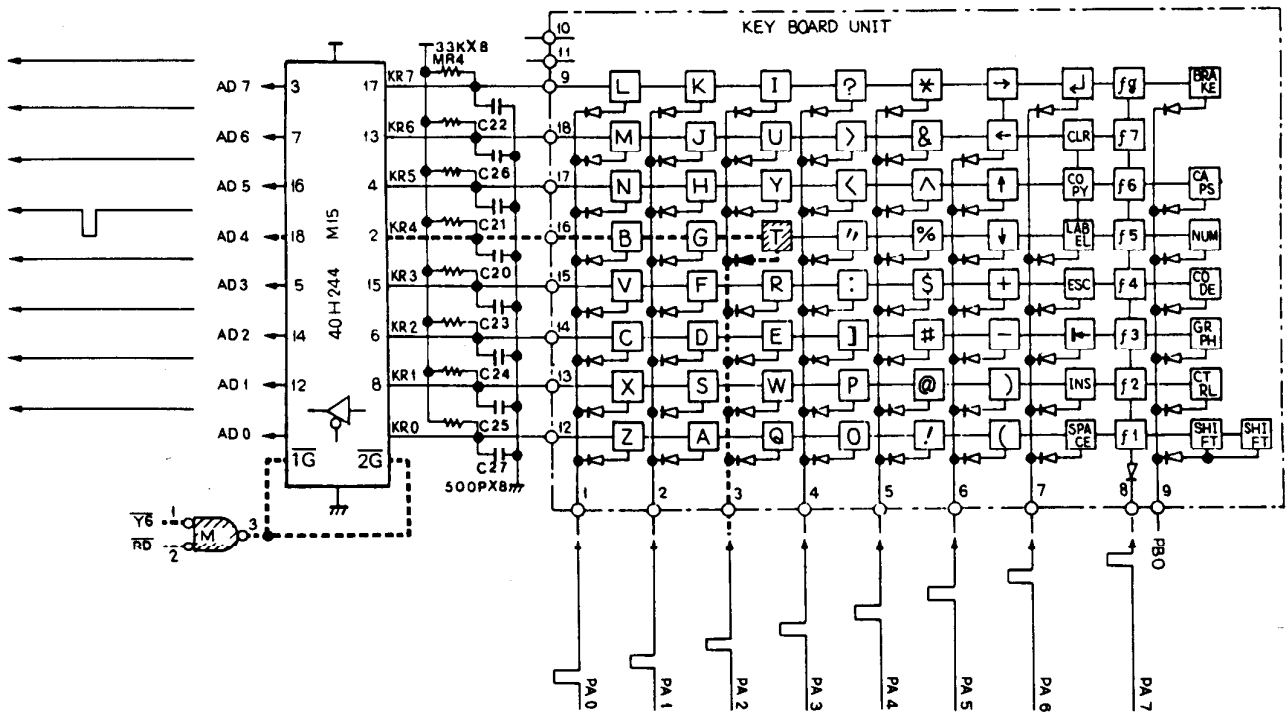
Figure 3-7. Control Circuitry (Condition of Pressing (T))

Cassette Interface Circuit

The cassette interface circuitry is divided into three sections:

- Modulation
- Demodulation
- Remote

In modulation, serial data is modulated and converted into a recording signal. The playback signal is demodulated and converted into a digital signal in demodulation. And, the remote is the part of the circuit that enables or disables the recorder's motor.

Modulation

Modulation is accomplished in several steps. First, serial data from the SOD terminal of the CPU is inverted (by M34). Next, the DC component is removed (by C63). Then, data passes through an integrator (consisting of R51 and C64) and, after voltage division, out to a recorder microphone input. Figure 3-8 shows the modulation circuit of the cassette interface.

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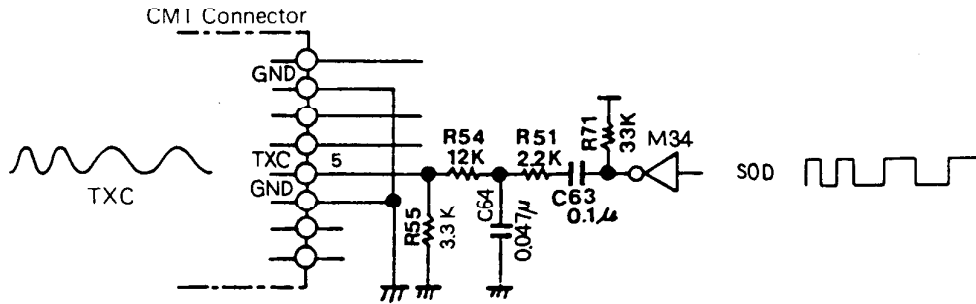
Figure 3-8. Modulation Circuit of Cassette Interface

Demodulation

The signal input from the earphone jack of the recorder passes through the D5 and D6 clamp circuit, and is then emitted from a comparator circuit composed of an operation amplifier IC (TL64, M30). The input signal is converted into a digital signal and applied to the SID terminal of the CPU. Figure 3-9 shows the demodulation circuit of the cassette interface.

In this circuit, D7 clamps the negative voltage output of the comparator.
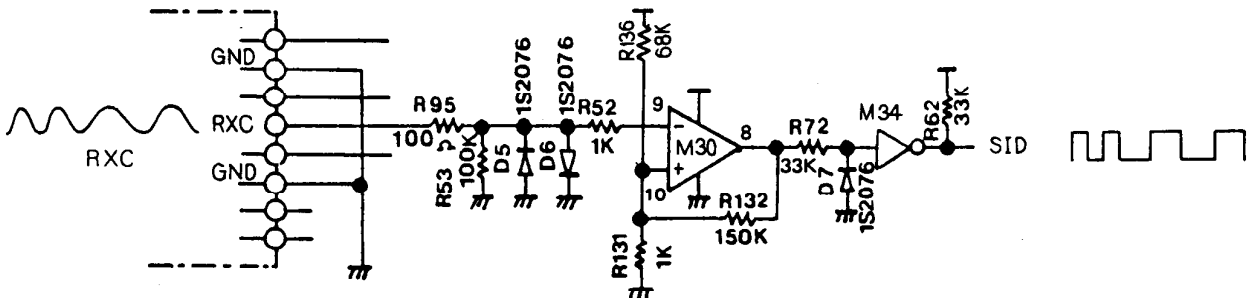
Figure 3-9. Demodulation Circuit of Cassette Interface

Remote

The REMOTE signal output is changed to L level as a result of the write-in of data 1 to bit 3 of the output port (40H175: M14) specified by I/O addresses E0H - EFH. As a result, T6 switches ON, the relay (RY1) is energized, and the recorder controls begin to operate. Figure 3-10 shows the remote circuit of the cassette interface.
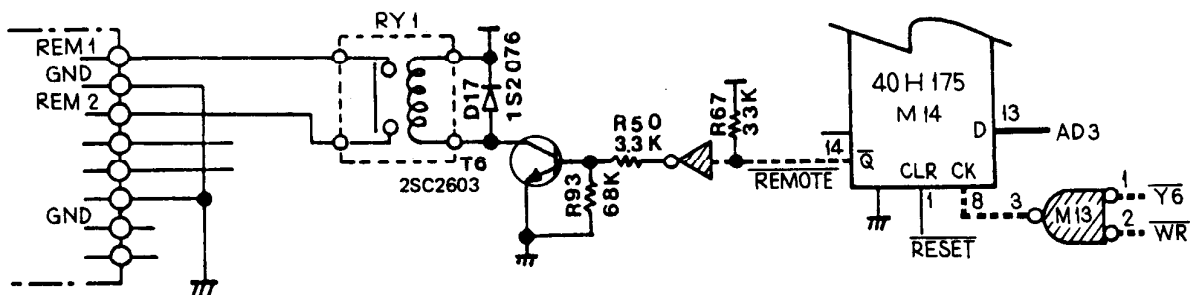
Figure 3-10. Remote Circuit of Cassette Interface

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Printer Interface

The printer interface circuit conforms to Centronics standards. As shown in Figure 3-11 below, the BUSY signal from the printer is read from PC2 of 81C55. If the condition is NOT BUSY (PC2: L level), the 8-bit data is sent to PA0 - PA7 of 81C55. Then, as a result of data 1 write-in to bit 1 of the output port (40H175: M14), indicated by I/O address E0H - EFH, T8 is switched ON and the L level $\overline{\text{STROBE}}$ signal is sent to the printer.

When the printer receives the $\overline{\text{STROBE}}$ signal, the BUSY signal is changed to H level, indicating that the printer is busy. The CPU then waits until the BUSY signal reaches the L level. When the BUSY signal reaches L level, the CPU ends the output of PA0 - PA7 data of 81C55, and the output of 1 byte of print data is completed.

If the printer is ON LINE, the $\overline{\text{BUSY}}$ signal is H level. But, if the printer is OFF LINE, the signal becomes L and transmission of print data to the printer is not possible.
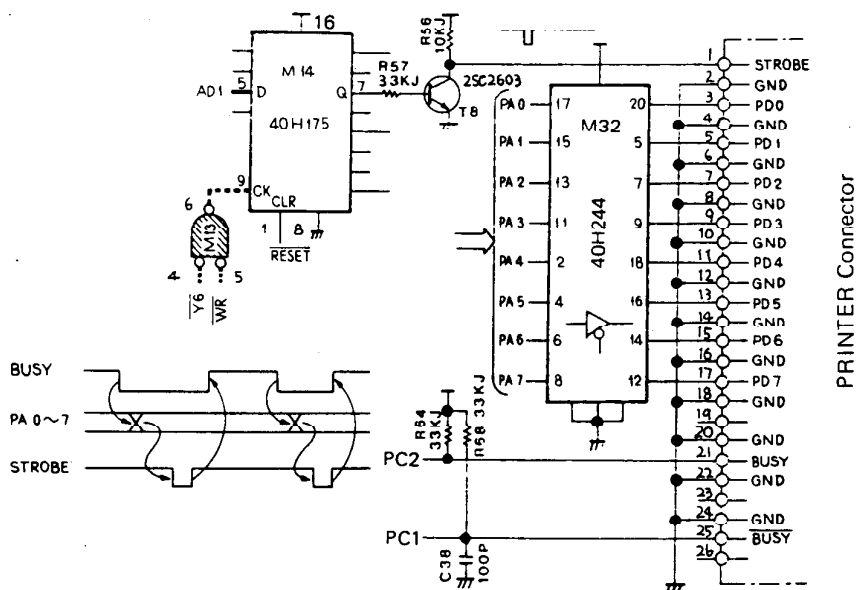
Figure 3-11. Printer Interface Circuit

Bar Code Reader Interface

The input signal from the bar code reader is subjected to waveform shaping, inverted by the Schmitt type inverter (M34), then delivered to the 81C55 PC3 and 80C85 RST 5.5 terminals.

When the bar code reader reads the first white part of the bar code, the L signal is generated, then inverted by M34. As soon as RST 5.5 interaction occurs, data input starts.

As the bar code reader is moved across the bar codes, H and L signals are generated to correspond to the white and black areas, respectively. Finally, the inversion signals are input to PC3 of 81C55 as serial data. Figure 3-12 shows the bar code reader interface circuit.

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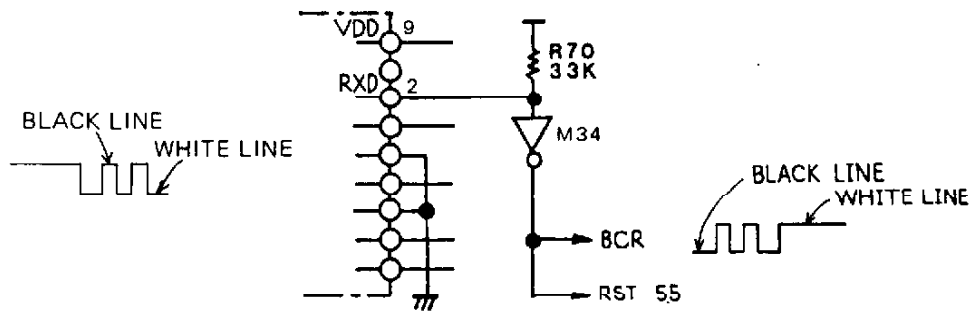
Figure 3-12. Bar Code Reader Interface Circuit

Buzzer Control Circuit

There are two ways to activate the buzzer. One is by emitting a signal from PB5 of 81C55 at a particular frequency; the other, by using the timer output of 81C55.

Signal from PB5 of 81C55

When PB2 of 81C55 is H level, the buzzer is made to sound by repeatedly switching the buzzer drive transistor ON and OFF. This is accomplished by the H, L, H, L . . . signals of output from PB5 synchronizing with the frequency for sounding the buzzer.

81C55 Timer Output

In this method, the buzzer is made to sound by setting the 81C55 timer in the square wave output mode and the value corresponding to the frequency which will sound the buzzer. With PB5 at H level, the buzzer will sound whenever PB2 is switched to L. This causes the square-wave pulse emitted from the timer out (TO) terminal of 81C55 to be applied to the base of the transistor for buzzer drive. PB2 uses this as the buzzer ON/OFF control signal.
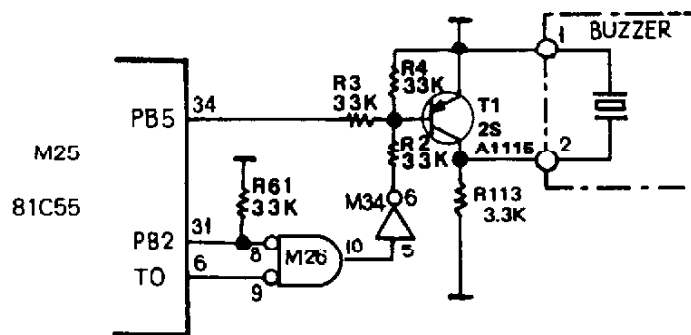
Figure 3-13. Buzzer Control Circuit

System Bus

To expand the use of external devices, the 40-pin system is made up of a 40-pin DIP IC Socket. As shown in Table 3-3, the 80C85 address bus, data bus, and control bus, can all be connected to the external system from the system bus, making system expansion easy. In addition, the optional I/O control unit and RAM file can be connected to this system bus.

Pin No.	Signal	Input or output	Pin No.	Signal	Input or output
1	VDD	—	40	VDD	—
2	GND	—	39	GND	—
3	AD0	In/output	38	AD1	In/output
4	AD2	In/output	37	AD3	In/output
5	AD4	In/output	36	AD5	In/output
6	AD6	In/output	35	AD7	In/output
7	A8	Output	34	A9	Output
8	A10	Output	33	A11	Output
9	A12	Output	32	A13	Output
10	A14	Output	31	A15	Output
11	GND	—	30	GND	—
12	$\overline{RD}$	Output	29	$\overline{WR}$	Output
13	IO/$\overline{M}$	Output	28	S0	Output
14	ALE	Output	27	S1	Output
15	CLK	Output	26	$\overline{Y0}$	Output
17	$\overline{Ⓐ}$	Output	25	$\overline{RESET}$	Output
27	INTR	Input	24	INTA	Output
18	GND	—	23	GND	—
19	RAM RST	Output	22	NC	—
20	NC	—	21	NC	—

(Note: NC - no connection)

Table 3-3. System Bus Pin Assignments

The following is an explanation of each signal in Table 3-3 with the exception of the CPU signal.

$\overline{Ⓐ}$ signal (pin 16)	NAND output signal of the $\overline{RD}$ signal and $\overline{WR}$ signal. Used by optional RAM file.
RAM RST signal (pin 19)	Enable signal (external C-MOS RAM). Used by optional RAM file.
$\overline{Y0}$ signal (pin 26)	Device-select signal of optional I/O controller unit

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Table 3-4 below shows the DC characteristics of each system bus signal.

Item	S0,S1,Y0,CLK	Other Signals
High-level output voltage (VOH)	2.4V min (IOH = −400μA)	4.95V min (IOH = −1μA)
Low-level output voltage (VOL)	0.45V max (IOL = 2mA)	0.05V max (IOL = 1μA)
High-level output current (IOH)	−400 μA min (VOH = 2.4V)	−0.8 mA min (VOH = 4.5V)
Low-level output current (IOL)	2 mA min (VOL = 0.45V)	4.0 mA min (VOL = 0.5V)
High-level input voltage (VIH)	—	4.0V min
Low-level input voltage (VIL)	—	1.0V max.

Table 3-4. System Bus DC Characteristics

Note: Values shown in Table 3-4 are for normal temperature (Ta = 25°C) and power (VDD = 5.0V).

LCD Interface Circuit

The LCD interface circuit links the LCD driver to the CPU. See Figure 3-14.

Figure 3-14. LCD Interface Circuit

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The following signals are necessary for LCD driver interface:

AD0 - AD7	For write-in of control data or display data to the LCD driver. Signal line for read-out from the driver.
Y7	LCD driver enable signal
PA0 - PA7, PB0, PB1	Chip enable signal for each LCD driver
S1	Indicates whether data is being written into the LCD driver (S1 = L) or read out (S1 = H)
A8	Register-select signal in the LCD driver. AD0 - AD7 data are display data when A8 = H; and command, or status data, when A8 = L.
E	NAND output signal of $\overline{RD}$ signal and $\overline{WR}$ signal. Indicates the timing of the LCD driver data read/write.
V2	Voltage to keep the LCD driver voltage standard. LCD display can be changed by changing the V2 voltage by VR2.

Figure 3-15 below shows the operating timing of each signal. Refer to the LCD PCB technical description for detailed characteristics and operation of the LCD and LCD driver.
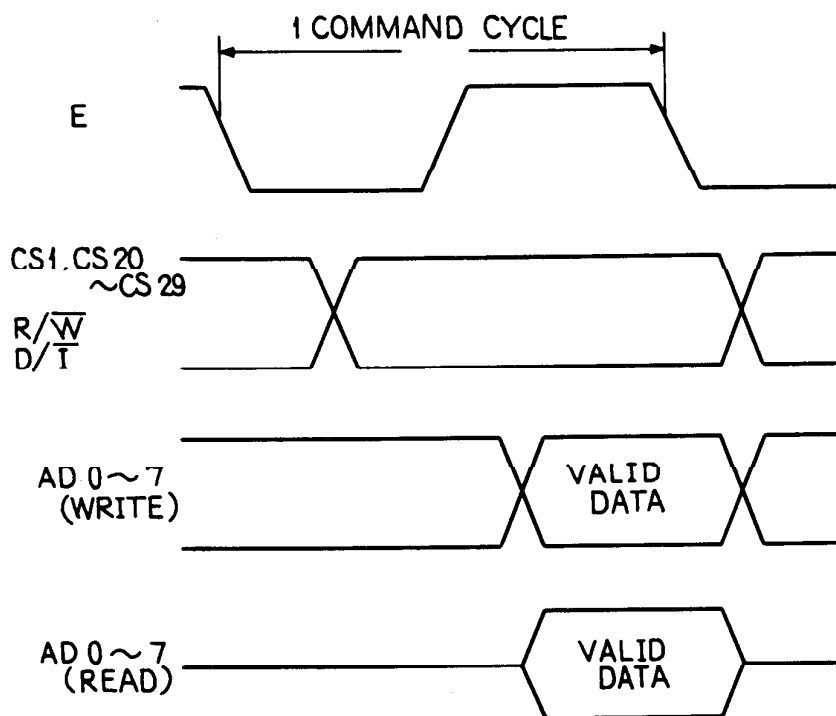
Figure 3-15. LCD Interface Timing Chart

Clock Control Circuit

A clock LSI (μPD1990AC) is used in the clock control circuit so that the time can be set and read through BASIC commands.

When the Model 100 is in the operable condition (RESET is H level), commands and data can be input and output to μPD1990AC (M18) from the CPU at will.

In addition, because battery voltage VB is applied to the μPD1990AC, the clock functions even when the Model 100's power switch is OFF.

The clock's LSI C0 - C2, DATA IN and CLK terminals are connected to the 81C55 PC0 terminal. The STB signal is provided from bit 2 of output port made by M14 (40H175).

The TP output signal is connected to the RST 7.5 interruption input terminal of the CPU. Square waves are output from the TP (4 ms cycle), and one key scan occurs every 4 ms because of the RST 7.5 interruption to the CPU.

Time Set Sequence

The CPU sets μPD1990AC to the register shift mode with the 100 pattern of C0 - C2 and the strobe signal which is generated by AD2, $\overline{Y6}$ and $\overline{WR}$ signals passing through M14. Then, the CPU sends the data of time and date information to the DATA IN terminal of μPD1990AC with timing clock (PA3). See Figure 3-16 below.
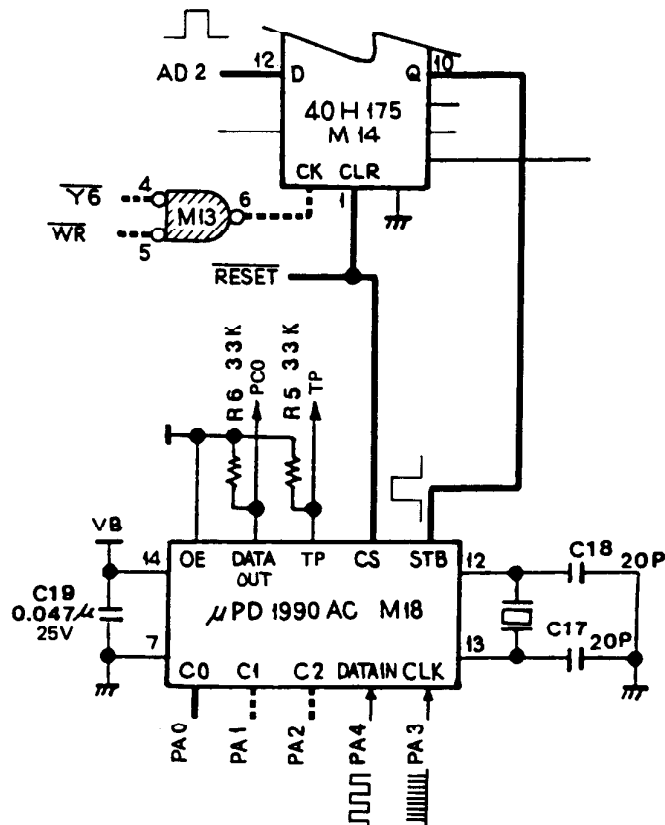
Figure 3-16. Data Input Condition of μPD1990AC

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Finally, the CPU sets the time set mode with the 010 pattern of C0 - C2 and the strobe signal. See Figure 3-17 below.

Figure 3-17. Time Set Condition of μPD1990AC

Time Read Sequence

The CPU sets μPD1990AC to the time read mode with the 110 pattern of C0 - C2, and the strobe signal. See Figure 3-18 below.

Figure 3-18. Time Read Condition of μPD1990AC

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The CPU sets to the register shift mode again with the 100 pattern of C0 - C2, and reads the data of time and data information from the DATA OUT terminal. At the same time, the CPU sends the PA3 signal passing through 81C55 for the timing clock.

Figure 3-19. Data Output Condition of μPD1990AC

Serial Interface Circuit

The serial interface circuit is divided into three parts — serial control, RS-232C interface, and modem. This circuit controls the changes and transmission/reception of data (parallel and serial data) between the CPU the modem and the RS-232C circuits.

Serial Control Circuit

Serial control is performed by the UART LSI (IM6402). The CPU begins data transmission/reception after the control word that determines the mode (transmission/reception) is written into the control register selected by the Y5 signal. See Figure 3-20.

Figure 3-20. Control Register Load Condition of IM6402

For transmission, the condition of the IM6402 TBRE signal from bit 4 of the status input port (M23), selected by the $\overline{Y5}$ signal, is read. If the signal is L, the chip waits until the signal becomes H. See Figure 3-21.

Figure 3-21. Status Read Condition of IM6402

When the TBRE signal becomes H, data transmission is possible. If the transmission data is written into the transmitter buffer register (TBR1 - TBR8), the data is output as serial data, containing the start, parity and stop bits from the TRO terminal. See Figure 3-22.
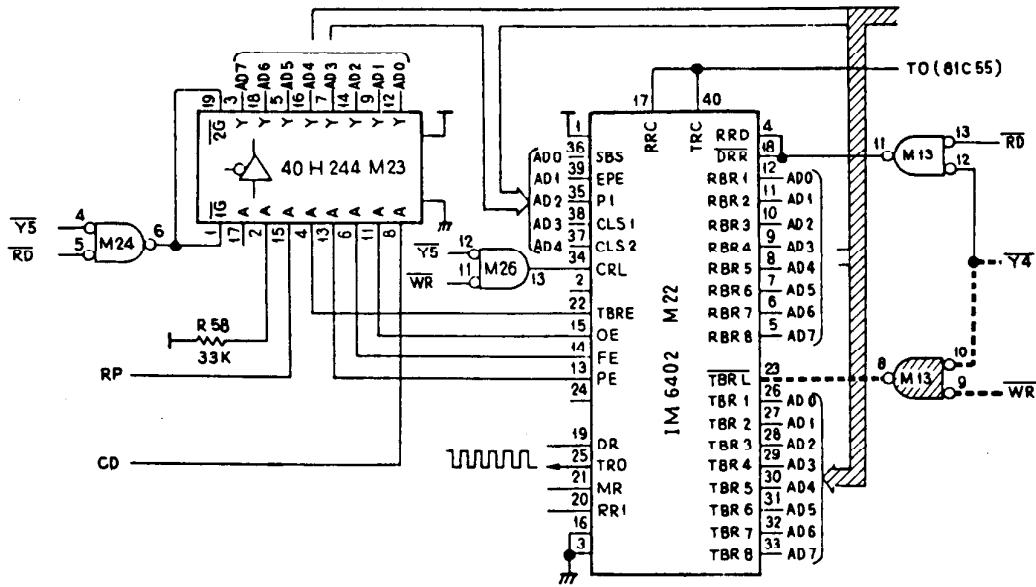
Figure 3-22. Data Transmission Condition of IM6402

For reception, when data enters the RRI terminal, the DR terminal changes from L to H and the RST 6.5 interruption notifies the CPU that reception data has entered IM6402. See Figure 3-23.
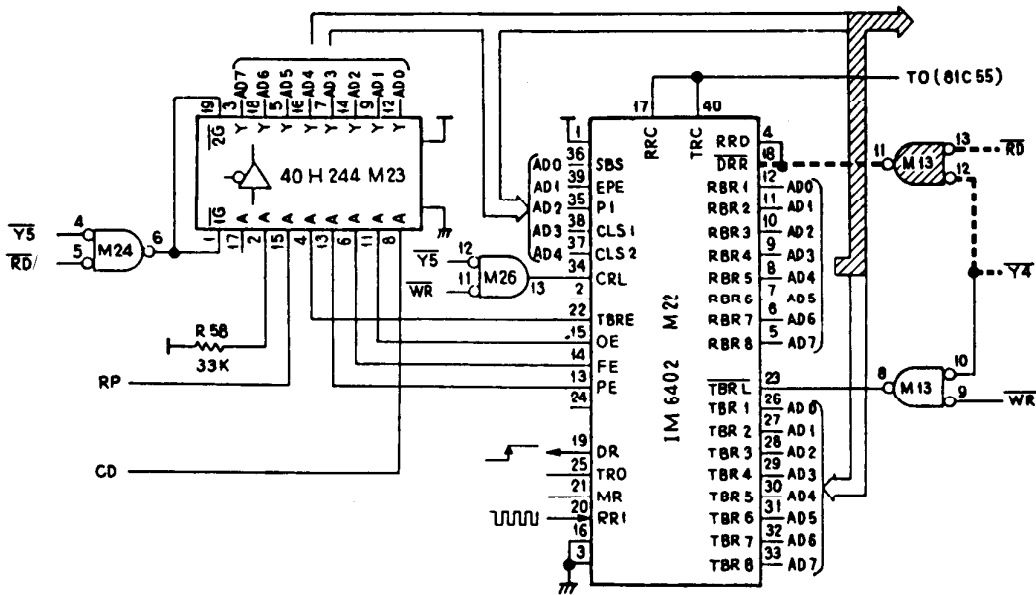
Figure 3-23. Data Reception Condition of IM6402.

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The CPU reads the OE, FE, and PE signals from the status input port (M23). If there is no error when the serial data is received, the reception data from the receive buffer register selected by $\overline{Y4}$ can be read as 8-bit parallel data.

The IM6402 serial transmission/reception reference clock signal is taken from the TO terminal by setting the 81C55 timer.

In addition, the status input port bit 5 RP signal is held as an option for MODEM operation.

Table 3-5 shows the signal correspondence between the data bus, status bit, and control register of IM6402.

Data bus	Control register	Status bit
AD0	SBS (Stop Bit Select)	—
AD1	EPE (Even Parity Enable)	OE (Overrun Error)
AD2	PI (Parity Inhibit)	FE (Framing Error)
AD3	CLS1 (Character Length Selected 1)	PE (Parity Error)
AD4	CLS2 (Character Length Selected 2)	TBRE (Transmitter Buffer Register Empty)
AD5	—	—
AD6	—	—
AD7	—	—

Table 3-5. Status Bit and Control Register of IM6402

MODEM/RS-232C Exchange Circuit

Because the serial input/output port which forms IM6402 is one channel only, the circuit shown in Figure 3-24 is multiplexed to $\overline{RS\text{-}232C}$ and the MODEM.

The $\overline{RS\text{-}232C}$ signal (PB3 terminal of 81C55) determines whether the serial port is to be used as RS-232C or as a Modem. When the $\overline{RS\text{-}232C}$ signal is L, the serial port is used as RS-232C. When it is H, the port is used as MODEM.

The reception signal, including the control signal, is demultiplexed at 40H157 (M33). The transmission signal is multiplexed at M24 and M26.

$\overline{CTS}$ and $\overline{DSR}$ signals (as the serial port) are input to PC4 and PC5 of 81C55. The CD signal is input from bit 0 of the status input port (M23). Output signals $\overline{DTR}$ and $\overline{RTS}$ are output from PB6 and PB7 of 81C55.

RS232C MODE   MODEM MODE
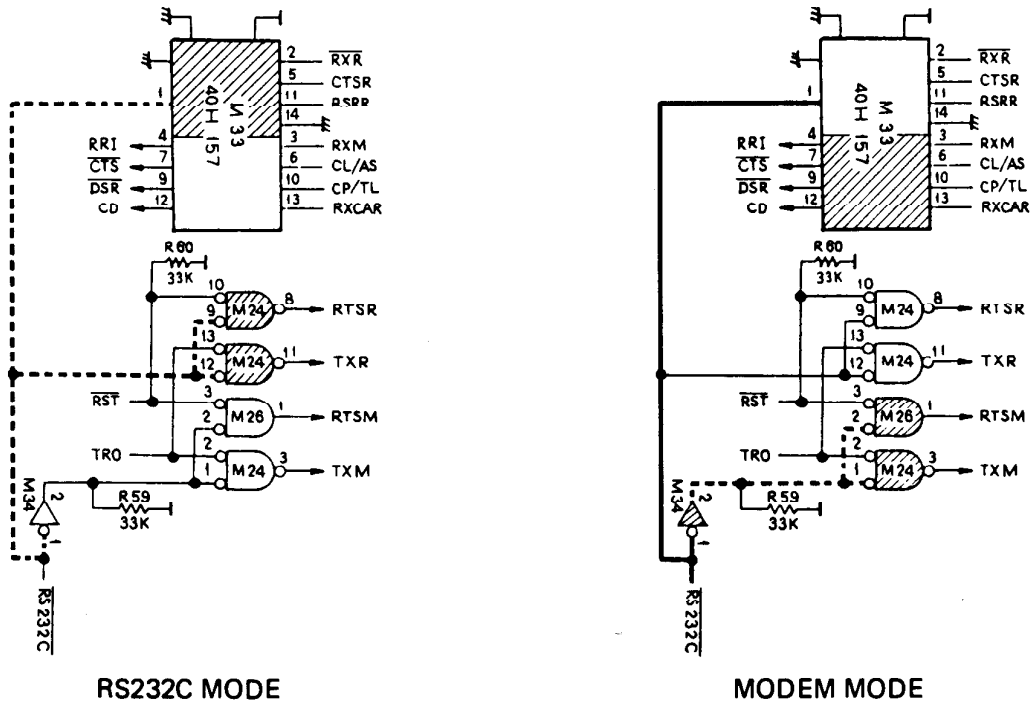
Figure 3-24. MODEM/RS-232C Exchange Circuit

RS-232C Interface Circuit

In the RS-232C transmission circuit, after the DC component is removed from the IM6402 TRO, $\overline{\text{RTS}}$, and $\overline{\text{DTR}}$ signals by the coupling capacitor (0.039 μF 50V), the signals are leveled to + −5V signals by the Schmitt trigger type inverter IC (M35), and then are output as RS-232C transmission signals.

In the RS-232C reception circuit, DSRR, CTSR, and RXR signals from the external RS-232C line are subjected to waveform shaping and inverted by M35 and diode IS1535, and then converted to +5V or GND level signals. The signals are then demultiplexed by 40H157 (M33) and converted to $\overline{\text{CTS}}$, $\overline{\text{DRS}}$, and RRI signals which can be controlled by the CPU. See Figure 3-25.

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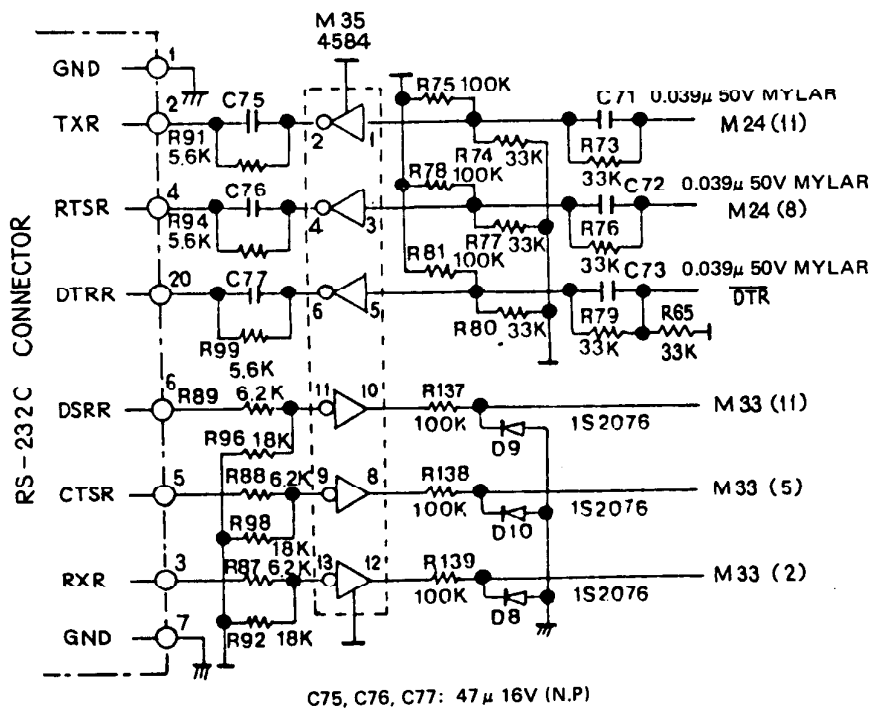
Figure 3-25. RS-232C Interface Circuit

Table 3-6 shows the application of each signal of the RS-232C circuit.

Symbol	Name	Application
TXR	Transmit Data	Data Output from RS-232C
RXR	Receive Data	Data Input to RS-232C
RTSR	Request to Send	
CTSR	Clear to Send	
DSRR	Data Set Ready	
DTRR	Data Terminal Ready	

Table 3-6. RS-232C Signals

Modulation/Demodulation LSI and Peripheral Circuit

Modem circuitry consists of the modulation/demodulation LSI, transmission filter, reception filter, and other circuits.

The Rx Rate and Type terminals of MC14412 (M31) are pulled up to VDD. Baud rate is set to 300 bps and the U. S. standard is selected. Since the ECHO and SELF TEST terminals are not needed, they are grounded. The Q output (En signal) of the port (M36) selected by bit 1 of the Y2 port is input to the ENABLE terminal until the unit is in the MODEM mode.

In addition, the signal designated by the ORIG/ANS switch is input to the MODE input, and switches between the Originate or the Answer mode. See Figure 3-26.

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(ORIGIN MODE)

Figure 3-26. MODEM LSI and Peripheral Circuit

Transmission Filter Circuit

The transmit carrier signal output from the Tx terminal is DC by C61. The signal level is adjusted to -26.5 dB by variable resistor VR2. The signal then passes through the transmission band-pass filter and is sent to the telephone line or the acoustic coupler.

The transmission circuit is composed of an active filter (consisting of an operational amplifier) and the intermediate frequency, which changes according to the mode (originate or answer).

Depending on the ORIG/ANS switch setting, transistor (T4) is ON or OFF, so that R42 is 2.3 K Ohms for the answer mode, and the synthesis resistance of the R42 and R45 values determines the originate mode.

The intermediate frequency of the active filter is 1,170 Hz for the originate mode, and 2,125 Hz for the answer mode. See Figure 3-27.

Figure 3-27. Transmission Filter Circuit

Reception Filter and Comparator Circuit

As shown in Figure 3-28a, the reception circuit input signal is amplified when passing through the coupling capacitor, and amplified again as it passes through the 3-stage band-pass filter (composed of an active filter). The signal then passes through the comparator, and after being changed to a square-wave, is input at the RX CAR terminal of MC14412.
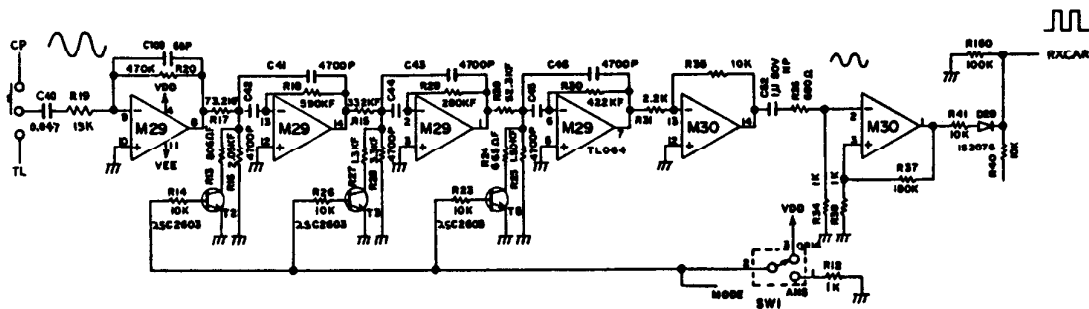
Figure 3-28a. Reception Filter and Comparator Circuit

Intermediate frequencies of the 3-stage active filter are shown below.

		1st stage	2nd stage	3rd stage
Intermediate Frequency	Originate Mode	980 Hz	1150 Hz	1330 Hz
	Answer Mode	1940 Hz	2120 Hz	2290 Hz
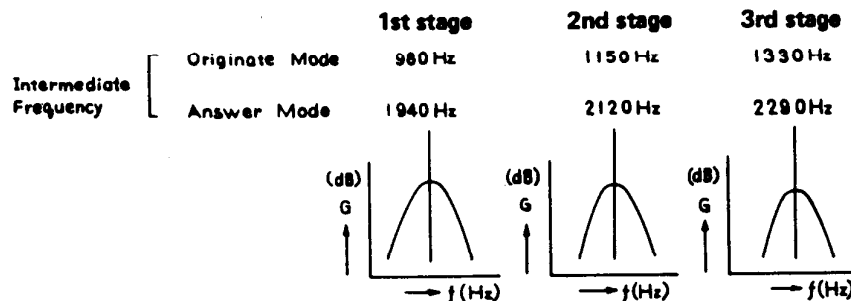
Figure 28b. Active Filter Frequencies

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LCD Panel

Liquid crystal is a substance midway between a liquid and a solid, although its appearance is much like a liquid. From an electrical and optical stand point, it possesses the properties of a crystal. Items using this substance are called liquid crystal display elements. The LCD used in Model 100 is a TN (Twisted Nematic) type of liquid crystal. Its basic construction is shown in Figure 3-30.
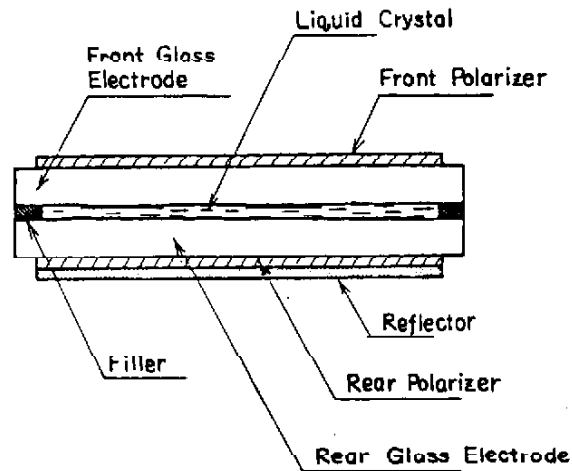
Figure 3-30. Construction of LCD Panel

The LCD operates as an "electric shutter" controlling the passage of light. That is, if voltage is applied, the transmission of light is blocked; otherwise light is allowed to pass.

Figure 3-31 demonstrates how the LCD operates:

1. The liquid-crystal display element is sandwiched between two polarization plates, with the polarized axes of the upper and lower plates positioned at right angles to each other.

2. As shown in Fig. 3-31 (a), when the liquid is not electrically excited, its long cigar-shaped molecules are parallel to each other and perpendicular to the plates.

3. In Fig. 3-31 (b), voltage is applied and the liquid appears frosted in current carrying areas. Ion activity causes the molecules to scatter incident light.

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Natural Light

Front Polarizer

Front Glass Electrode

OFF

Twisted 90°

ON

Rear Glass Electrode

Rear Polarizer

Reflector

Light is passed   Light is interrupted
Bright   Dark
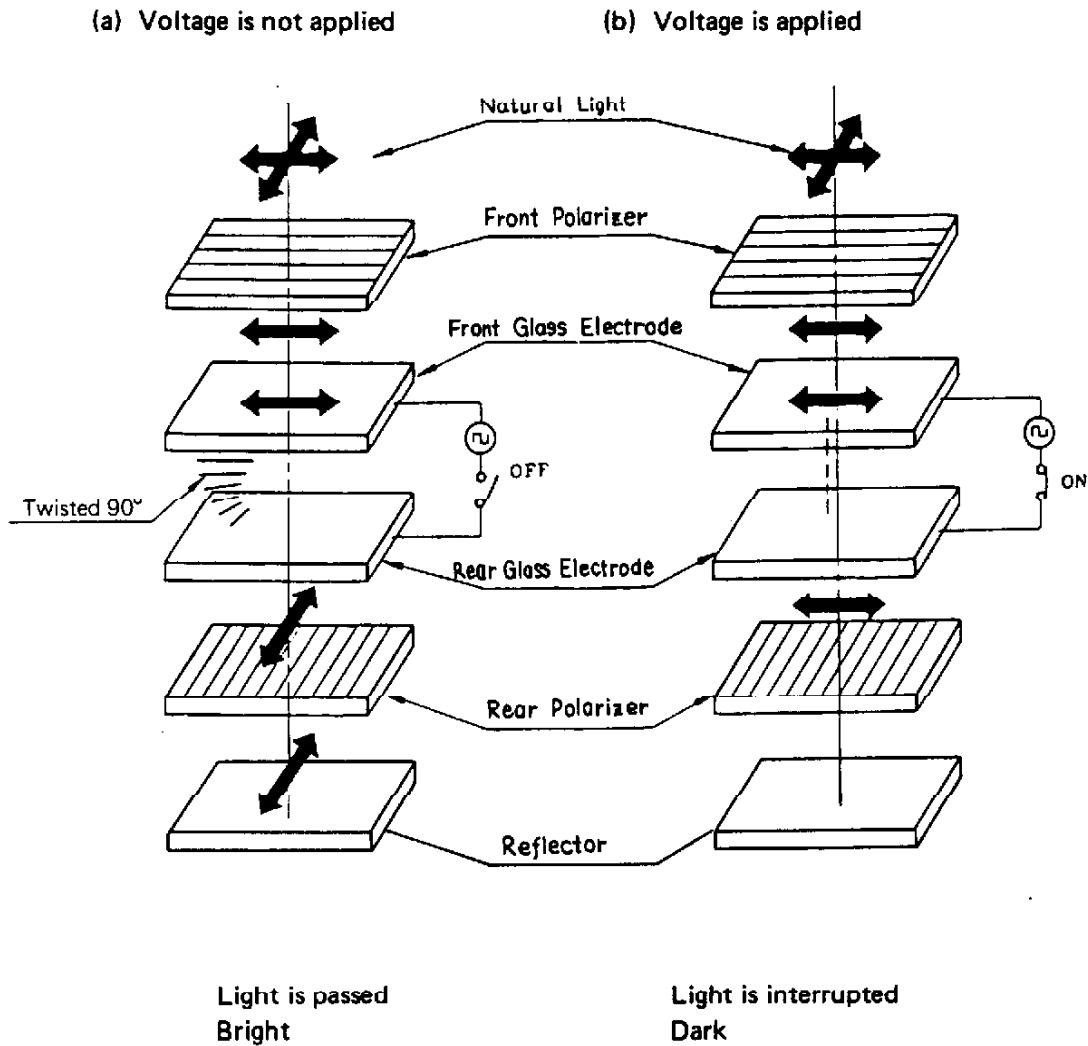
Figure 3-31. Operation Theory of LCD Panel

The LCD used in Model 100 is composed of electrodes in a matrix arrangement (back scan 64, segments 480). Refer to Figure 3-32. Because the LCD operates on a 1/32 duty time-division drive, the upper 32 and lower 32 back scanning is performed by the same signal.
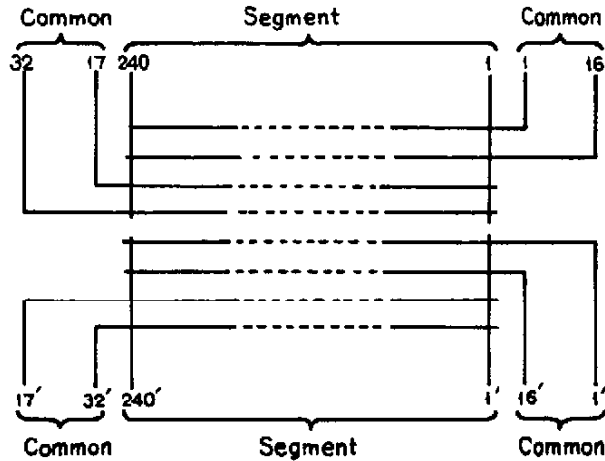
Figure 3-32. LCD Electrodes

The angle of the field of vision is 30° in the range that contrasts. K = 1.4 or more (brightness of non-illuminated segment divided by the brightness of illuminated segment). This range can be set by adjusting the LCD drive voltage with the Display Control Dial.
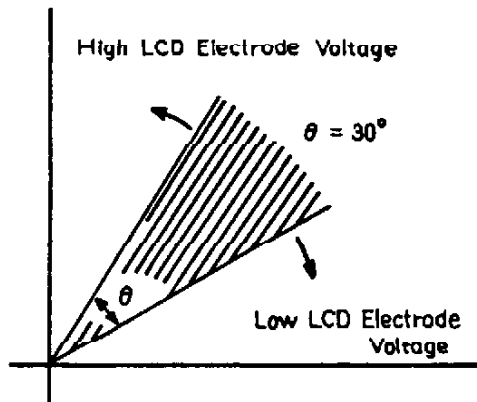
Figure 3-33. LCD View Angle

Caution: The polarization plate attached to the surface of the LCD panel is scratched very easily, and must be handled with great care.

To clean contacts or the display surface, dampen a soft cloth slightly with benzine and wipe gently. Do not use organic solvents such as alcohol.

LCD Control Circuit

Refer to the LCD PCB diagram, Figure 3-34, while reading this section.

ICs M11 and M12 (HD44103) are back-scan driver ICs. The timing signal necessary for the display is generated by the built-in oscillator, C5, and R10. This timing signal is also supplied to the segment driver for control of the display.

There are 16 HD44103 back-scan signal outputs. M11 and M12 are cascade connected, and a 1/32 duty back-scan signal is made. By using a C and R only at the M11 side, a timing signal is generated which controls M12. M11 can then be considered as the master IC and M12, the slave. The basic oscillation frequency is about 430kHz. Figure 3-34 shows the internal logic composition.
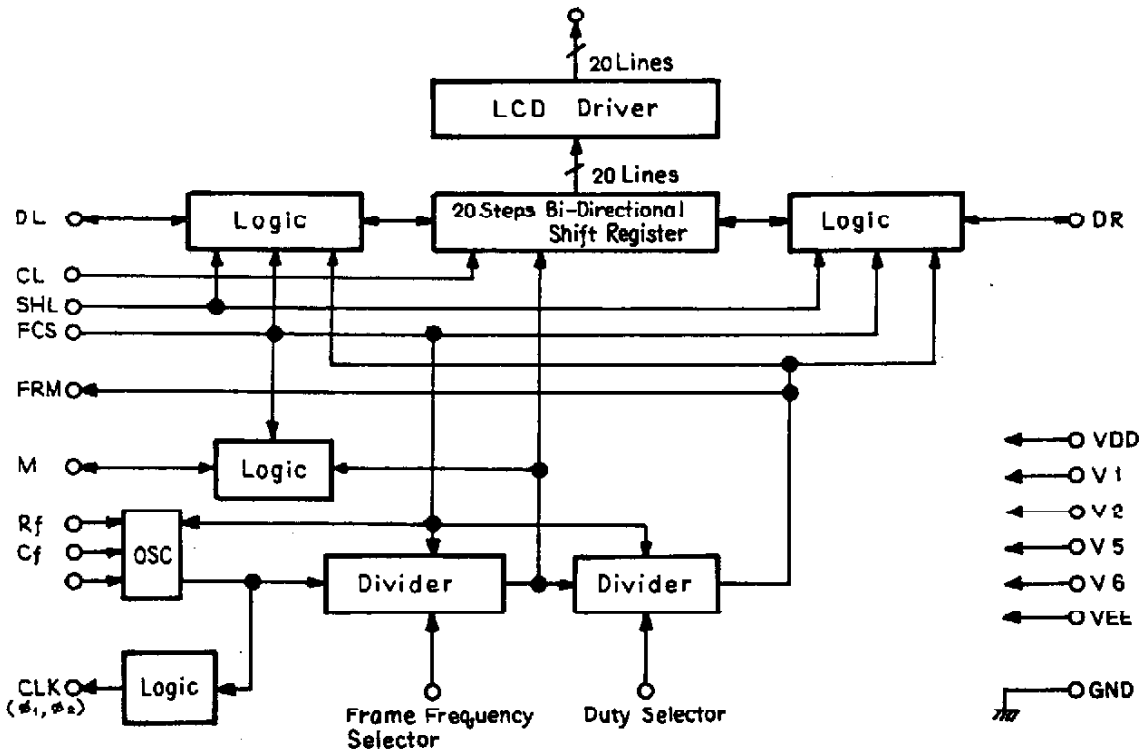
Figure 3-34. HD44103 Internal Logic Diagram

The timing signals are M, FRM, CLK (ϕ_1, ϕ_2), and CL. The M signal inverts the LCD drive waveform one image at a time to change it to AC. Since continuous application of DC to the LCD shortens the element life, an alternating electric field is applied to the liquid-crystal surface during drive to make the waveforms symmetrical and reduce the DC component.

The FRM signal is the display repeat frequency which sets the number of scans per second. For the Model 100, FRM ≃ 70 Hz.

The ϕ_1, and ϕ_2 signals are the locks for HD44102 RAM operation.

The CL signal is the shift clock for the shift register.

ICs M1 - M10 (HD44102) are segment driver ICs that cause the display data sent from the CPU board to be memorized in the built-in RAM and automatically generate the liquid-crystal drive signal.

One bit of data from the built-in RAM corresponds to one dot of illumination or non-illumination on the display. The driver output is 50 lines. The transfer of the data is accomplished by 8-bit parallel data. This IC has several types of commands and the D/I (H: data, L: command) signal distinguishes between commands and data. Figure 3-35 shows the internal logic composition.
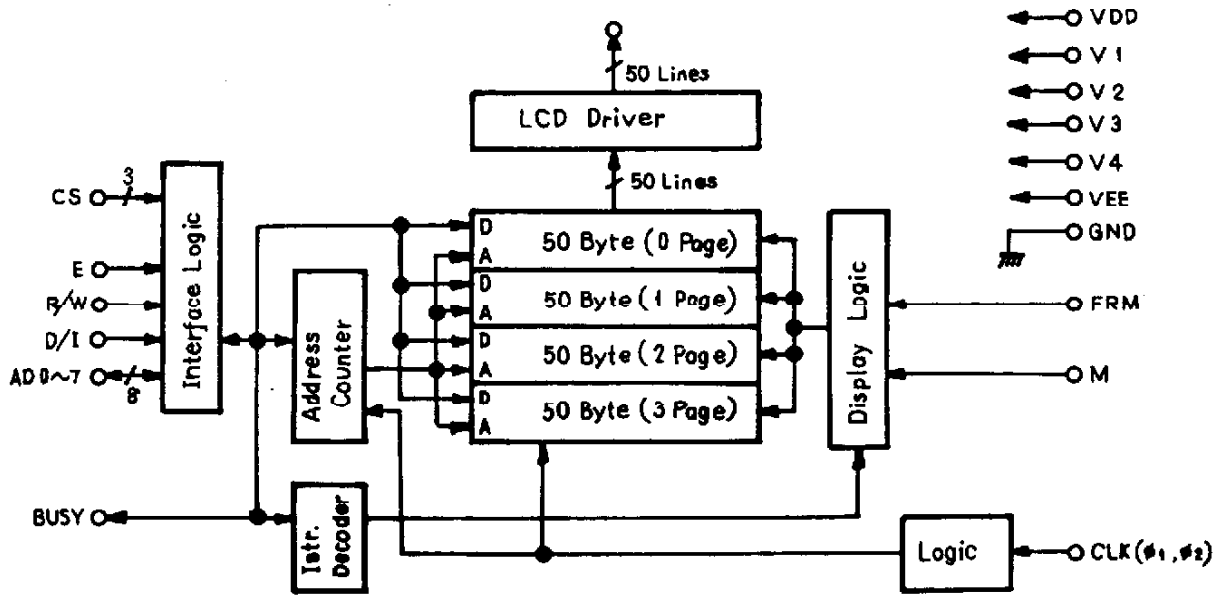
Figure 3-35. HD44102 Internal Logic Diagram

Because Model 100 has 240 segments each (upper and lower), the M5 and M10 segment output Y41 - Y50 becomes NO-CONNECTION. The power supplied to these ICs, in addition to VDD (+5V) and VEE (−5V), includes V1 - V6.

VDD and VEE are the power supplies which operate the IC logic, and V1 - V6 make up the LCD signal. V1 - V6 are made up by the resistance splitting of R1, R2, R3, R4, and R5. By passing through operation amplifier M13 (HA17902), the output impedance of the power supply is lessened. Capacitors C3, C4, C6, C7, and C8 increase the peak current during LCD illumination. R11, R12, and R13 are resistors for IC latch-up prevention.

This board also includes a low-power detection LED and buzzer connectors.

LCD Waveform

To drive the liquid-crystal elements by the 1/32 duty line-sequential drive method, the LCD of the Model 100 makes sequential selection of the 32 scanning electrodes. For each dot, the display signal passes through the signal electrodes and is applied 32 times for one display. At this point, the signal is necessary at each dot only one time, and the signals for the other 31 times correspond to other dots on the same signal electrode.

The maximum voltage applied to the Common electrode and Segment electrode is the potential difference between V1 and V2.

In addition, a is the bias coefficient which determines, from the standpoint of contrast, the maximum ratio between the illumination and the non-illumination voltage.

When that ratio is greatest in relation to the effective ON and OFF voltages, $a = 6.66$. Thus, for V1, V2, V3, V4, V5, and V6:

$$V1 = VEE (-5V)$$
$$V2 = V (About\ 0 \sim 4V)$$
$$V3 = 2/aV$$
$$V4 = (1 - 2/a)V$$
$$V5 = (1 - 1/a)V$$
$$V6 = a/aV$$

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Figure 3-36 shows the drive waveform for illumination and non-illumination.
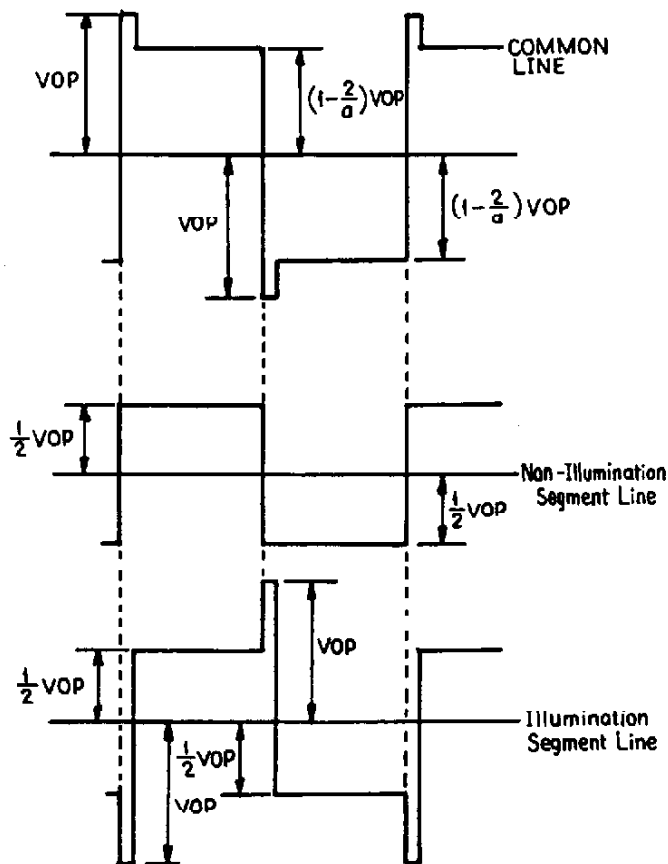
Figure 3-36. LCD Waveform

Power Supply and Auto-Power OFF Circuit

The power required by the logic circuits of Model 100 is ±5V, supplied by the DC/DC converter.

A special feature of Model 100 is the Automatic Power OFF function. This circuit will be described in three parts: first, the circuit which supplies the power; secondly, the low-power detection and automatic power OFF circuits; and lastly, the reset circuit.

DC/DC Converter Circuit

OT2 is a converter transformer which oscillates T21 and T22 and generates voltage at the secondary side of the transformer. When the power is switched ON, a slight collector current flows to T21 and T22. A voltage between pins 7 and 9 of the converter transformer is generated, and the T22 base potential becomes positive. In other words, the base polarity becomes biased in the forward direction. This voltage causes the T21 and T22 base current to flow, and the collector current is increased.

When the collector current can no longer increase, because of transistor saturation resistance and converter coil resistance, the voltage between pins 7 and 9 begins to attenuate. As a result, the base current and collector current also attenuate, cutting off T21 and T22 due to the reverse bias action.

Until immediately before the transistor is cut off, an excitation current flows to the transformer. Since the current is suddenly cut off as a result of transistor cut-off, a counter voltage is generated, the distributed capacity of the coil is charged, and an oscillation voltage is generated at the base coil.

When the base potential reaches a half cycle of the oscillation voltage, it is biased in the forward direction and T21 and T22 are switched ON again. Oscillation occurs as shown in Figure 3-37.

5V/DIV
5μSec/div
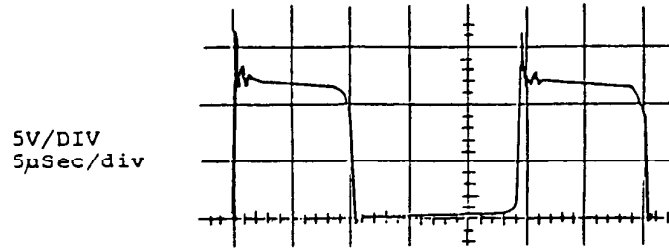
Figure 3-37. Oscillation Waveform

In this way, AC voltage corresponding to the number of windings is generated at the secondary side of the converter. The voltage is rectified and smoothed by D13, D15, C84, and C85.

Voltage fluctuations of VDD (+5V) are fed back to the primary side of the oscillation transistor by T13, D4, R121, and C92 to improve stability. C81 and R126 are a differentiation circuit designed to make the playback operation of the oscillation transistor easier. AC shorts the circuit so that the oscillation frequency is affected by the time-constant of this C and R. Since feedback is applied by VDD (which makes stability difficult), VEE (−5V) is further stabilized by R97 and D14. (The voltage at both ends of C85 is about −7V). See Figure 3-38.
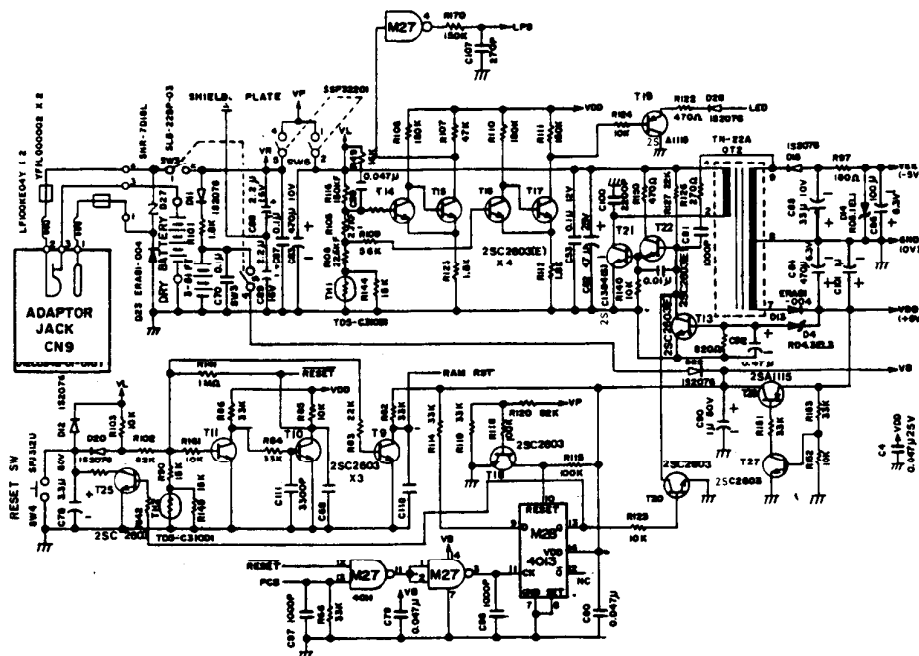
Figure 3-38. Power Supply and Reset Circuit

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Low-Power Detection and Automatic Power Off Circuit

The low-power detection circuit illuminates an LED warning lamp when the battery voltage decreases. If it continues to decrease, the system power will switch off just before the voltage falls too low for the converter to operate. There will be about 20 minutes between the time the LED lamp illuminates and the system is switched off, provided there are no I/O devices connected.

Battery voltage is detected by splitting the resistance of R144, R108, R105, and R116. When battery voltage (VL) becomes 4.1V ± 0.1V, T16 is switched off, T17 is switched on, T19 is driven, and the LED illuminates. (The LED is located on the LCD PCB.)

When VL becomes 3.7V ± 0.1V, T14 is switched off, T15 is switched on, and LPS changes from H to L. This signal is inverted by M27 and fed to the TRAP terminal of 80C85. If the CPU acknowledges this signal, the P.C.S. signal is sent, passing through the PB4 of 81C55 after the internal operations.

The P.C.S. signal is active H. When P.C.S. becomes H, the Q output of M28 (4013: D type F/F) becomes H, T20 operates, and the oscillation of the converter is stopped.

If there is no operation for 10 minutes or more (awaiting a command for 10 minutes or more), P.C.S. is output from PB4 of 81C55.

When the power switch is switched OFF, T18 is switched OFF, the M28 RESET terminal becomes L and oscillation is resumed by turning the power switch ON. If the power is reduced by the LPS signal, battery replacement is necessary. R123 and R112 are resistors to provide hysteresis.

Reset Circuit

This circuit supplies the CPU $\overline{\text{RESET}}$ signal and also the RAM RST signal as the RAM protecting signal when the power decreases. The circuit diagram is shown in Figure 3-38.

R103 and C78 delay the introduction of input power so that T11 is switched ON and T10 is switched OFF after VDD is activated. As a result, the $\overline{\text{RESET}}$ signal changes from L to H. The RAM RST signal is generated by T9 and changes from H to L.

R141 provides hysteresis to the $\overline{\text{RESET}}$ signal. Thermistor TH2 suppresses $\overline{\text{RESET}}$ signal fluctuations due to temperature. T25 receives the signal during automatic power-off, short-circuiting both ends of C78, and resets the system.

The $\overline{\text{RESET}}$ signal is active L and RAM RST signal is active H.

Section 4. Preventive Maintenance

Model 100 requires very little maintenance care. Since the unit is completely aligned and adjusted at the factory, no electrical or mechanical modifications are necessary.

Cleaning the Body and LCD Display

Always keep the computer clean to prevent any operational malfunction. The body and LCD can easily be cleaned with a soft, dry, lint-free cloth. For tough stains, slightly dampen the cloth with benzol. Do not use solvents other than benzol for cleaning.

Section 5. Troubleshooting

This section shows you how to solve a problem or malfunction that has been identified. After locating the problem in the Troubleshooting Flowchart, turn to the section indicated by the number at the right. That section then identifies the components associated with the circuit in question and provides remedial instructions.

When the repairs are completed, you should re-check each functional item by the **Check List** provided. The Check List can also be used even if the location and condition of the malfunction are not readily clear.

Troubleshooting Flowchart Guide

START

Doesn't work at all? — NO → 1
YES

LCD doesn't function? — NO → 2
YES

Keys don't function? — NO → 3
YES

Buzzer doesn't function? — NO → 4
YES

Clock doesn't function? — NO → 5
YES

RESET doesn't function? — NO → 6
YES

Memory protection doesn't function? — NO → 7
YES

A

```
                              ┌───┐
                              │ A │
                              └───┘
                                │
                                │
            ◇─────────────────────────────────────◇      NO      ┌───┐
              Printer interface doesn't function?     ──────────▶ │ 8 │
            ◇─────────────────────────────────────◇              └───┘
                               YES
                                │
            ◇─────────────────────────────────────◇      NO      ┌───┐
              Cassette interface doesn't function?    ──────────▶ │ 9 │
            ◇─────────────────────────────────────◇              └───┘
                               YES
                                │
            ◇─────────────────────────────────────◇      NO      ┌────┐
              B.C.R. interface doesn't function?      ──────────▶ │ 10 │
            ◇─────────────────────────────────────◇              └────┘
                               YES
                                │
            ◇─────────────────────────────────────◇      NO      ┌────┐
              RS-232C interface doesn't function?     ──────────▶ │ 11 │
            ◇─────────────────────────────────────◇              └────┘
                               YES
                                │
            ◇─────────────────────────────────────◇      NO      ┌────┐
              MODEM interface doesn't function?       ──────────▶ │ 12 │
            ◇─────────────────────────────────────◇              └────┘
                               YES
                                │
            ┌─────────────────────────────────────┐      NO      ┌────┐
            │       All functions check OK?        │   ─────────▶ │ 13 │
            └─────────────────────────────────────┘              └────┘
                                │
                         ╭──────────────╮
                         │     END      │
                         ╰──────────────╯
```

Recommended Procedures

1. Model 100 doesn't work at all.

(1)

↓

Check the power
- Check to be sure that the batteries are in and that the AC adapter is connected.
- Is the memory back-up power switch ON?
- Is the power switch ON?

↓

Check the DC/DC converter circuit.
- Is 3.6—3.8V applied to pin 1 of the converter transformer?
  (If not, check C82, C83, battery contacts and adapter jack.)
- Check all output voltages.
  a) VDD . . . +5V (if not, check D13, C84 and D4)
  b) VEE . . . −5V (if not, check D15, C85 and D14)
  c) VB . . . . +5V (if not, check T27 and T28)
- Is T21 oscillating?
  (If not, check T22, T13, C81, R126, R127, R140 and T20.)

↓

Check the RESET signal.
- Is signal high level (+2.2V −5.3V)?
  If not, check T10, T11, T25, T9 RESET signal.
- Is signal low level (0.8V −0.3V)?
  If not, check T10, T11, T25, T9 RESET signal.

↓

Check the logic circuit.
- Check the CPU clock frequency.
  (X1 terminal = 4.9152 MHz; CLK terminal = 2.4576 MHz)
  (If not, check X2 and M19.)
- Try replacing the LCD unit.
- Check all IC s.

↓

(END)

2. LCD doesn't function.

```
              ( 2 )
                │
                ▼
        ╱ No display at all ╲   NO
        ╲                   ╱ ─────────────┐
                │ YES                      │
                ▼                          │
  ┌──────────────────────────────────┐    │
  │ Check source voltage (VDD, VEE, VB). │ │
  │ Refer to (1) "Doesn't work at all". │ │
  └──────────────────────────────────┘    │
                │                          │
                ▼                          │
  ┌──────────────────────────────────┐    │
  │ Check the RESET signal.           │    │
  │ Refer to (6) "Reset doesn't function". │ │
  └──────────────────────────────────┘    │
                │ ◄────────────────────────┘
                ▼
  ┌──────────────────────────────────────────────┐
  │ Check the LCD waveform.                        │
  │ (If abnormal, check the LCD power supply operation amplifier.) │
  └──────────────────────────────────────────────┘
                │
                ▼
  ┌──────────────────────────────────────────────┐
  │ Check the interface circuitry.                 │
  │ (Check all IC's connected to the bus line, M17 and M25.) │
  └──────────────────────────────────────────────┘
                │
                ▼
  ┌──────────────────────────────────────┐
  │ Check if connector is correctly connected. │
  └──────────────────────────────────────┘
                │
                ▼
  ┌──────────────────────────────────────────────┐
  │ Check LCD drivers (on LCD PCB) HD44102 and HD44103. │
  │ (Or replace the LCD unit.)                     │
  └──────────────────────────────────────────────┘
                │
                ▼
        (      END      )
```

3. Keys don't function.

```
        (3)
         │
┌────────┴────────────────────────────────┐
│ Check if keyboard connector is correctly connected. │
└────────┬────────────────────────────────┘
         │
┌────────┴──────────────────────────────────────────────────────────────┐
│ Check the key scan signal.                                              │
│ Is scan signal present at M25 PA0 — PA7 and PB1?                        │
│ (If not, check if pulses are emitted from the TP terminal (pin 10) of M18 and M25 at 4 msec │
│ intervals.)                                                             │
└────────┬──────────────────────────────────────────────────────────────┘
         │
┌────────┴──────────────┐
│ Check diodes on keyboard. │
└────────┬──────────────┘
         │
┌────────┴──────────┐
│ Check the return signal. │
└────────┬──────────┘
         │
┌────────┴──────────────────────────────┐
│ Check M15, M13, M16 and pull-up resistor MR4. │
└────────┬──────────────────────────────┘
         │
┌────────┴──────────────────────────┐
│ Check the key switching no-input keys. │
└────────┬──────────────────────────┘
         │
     (  END  )
```

4. Buzzer doesn't function.

```
        (4)
         │
      ╱──┴──╲                    NO
     ╱ Beep is ╲──────────────────────────────┐
     ╲ heard.  ╱                               │
      ╲──┬──╱                                  │
         │ YES                                 │
┌────────┴──────────────────────────────────┐ │
│ Check connector connections.               │ │
│ ● Check if LCD connector is correctly connected. │ │
│ ● Check if buzzer connector on LCD PCB is correctly connected. │ │
└────────┬──────────────────────────────────┘ │
         │◄─────────────────────────────────────┘
┌────────┴──────────────────────────────────┐
│ Check buzzer control logic.                │
│ Check M26, M34 and M25 (PB5 port, TO terminal). │
└────────┬──────────────────────────────────┘
         │
┌────────┴────────┐
│ Check the buzzer. │
└────────┬────────┘
         │
     (  END  )
```

50

5. Clock doesn't function.

```
        ( 5 )
          │
          ▼
┌──────────────────────────────────────┐
│ Check the power supply voltage.        │
│ ● When power ON:      +5V              │
│ ● When power OFF:     2.0 − 4.0V       │
│   (If not normal, check power supply circuit.) │
└──────────────────────────────────────┘
          │
          ▼
┌──────────────────────────────────────┐
│ Check oscillation frequency (f = 32.768 kHz). │
│ (If not normal, check X1, C17, C18 and M18.) │
└──────────────────────────────────────┘
          │
          ▼
┌──────────────────────────────────────┐
│ Check that a 250-Hz pulse is output from TP signal. │
└──────────────────────────────────────┘
          │
          ▼
┌──────────────────────────────────────┐
│ Check clock-setting ICs (M14 and M25) and RESET signal. │
└──────────────────────────────────────┘
          │
          ▼
      (  END  )
```

6. Reset doesn't function.

```
        ( 6 )
          │
          ▼
┌──────────────────────────────────────┐
│ Check RESET circuit.                   │
│ (Check T11, T10, T9, T25, D20, D22 and C78.) │
└──────────────────────────────────────┘
          │
          ▼
┌──────────────────────────────────────────────────┐
│ Check all ICs which have RESET and RESET signals.  │
│ (Check M19, M25, M22, M14, M27, M36 and M31, and also check LCD unit and RAM.) │
└──────────────────────────────────────────────────┘
          │
          ▼
      (  END  )
```

7. Memory protection doesn't function.

```
        ( 7 )
          │
          ▼
┌──────────────────────────────────────────────────────────────────────┐
│ Check power supply voltage.                                            │
│ ● When power ON:      VB = +5V (if not, check converter circuit)       │
│ ● When power OFF:     VB = 2.0 − 4.0V (if not, check Ni-Cad battery, D11 and D22) │
└──────────────────────────────────────────────────────────────────────┘
          │
          ▼
┌──────────────────────────────────────────────────────────────────────┐
│ Check to be sure that there is no deviation in the timing of the signal and that the level changes │
│ symmetrically, when the RAM RST and RESET are switched ON/OFF.         │
└──────────────────────────────────────────────────────────────────────┘
          │
          ▼
┌──────────────────────────┐
│ Check CMOS RAM.          │
└──────────────────────────┘
          │
          ▼
      (  END  )
```

8. Printer Interface doesn't function.

```
        ( 8 )
          │
          ▼
┌──────────────────────────┐
│ Check the strobe signals.│
│ Check M14 and T8.        │
└──────────────────────────┘
          │
          ▼
┌──────────────────────────┐
│ Check the data signals.  │
│ Check M25 and M32.       │
└──────────────────────────┘
          │
          ▼
┌──────────────────────────────────────┐
│ Check the connector and printer cable.│
└──────────────────────────────────────┘
          │
          ▼
      (  END  )
```

9. Cassette Interface doesn't function.

```
         ( 9 )
           │
           ▼
┌──────────────────────────────────────────────────────────────────────┐
│ Check TXC signals.                                                     │
│ Is a modulated waveform output to pin 5 of the cassette connector during program (DATA) │
│ save?                                                                  │
│ (If not, check M34, M19, C68 and C64.)                                 │
└──────────────────────────────────────────────────────────────────────┘
           │
           ▼
┌──────────────────────────────────────────────────────────────────────┐
│ Check RXC signals.                                                     │
│ Is a digital waveform input to the SID terminal of the CPU during program (DATA) load? │
│ (If not, check D5, D6, M30, M34 and M19.)                              │
└──────────────────────────────────────────────────────────────────────┘
           │
           ▼
┌──────────────────────────────────────────┐
│ Check the remote circuit.                 │
│ Check the relay (RY1), T6, M34 and M14.   │
└──────────────────────────────────────────┘
           │
           ▼
┌──────────────────────────────────────────────────┐
│ Check the cassette connector and cassette cable.  │
└──────────────────────────────────────────────────┘
           │
           ▼
      ( END )
```

10. B.C.R. Interface doesn't work.

```
         ( 10 )
           │
           ▼
┌────────────────────────────┐
│ Check M34, M25 and M19.     │
└────────────────────────────┘
           │
           ▼
┌──────────────────────────────────────────┐
│ Check the power supply voltage VDD (+5V).  │
└──────────────────────────────────────────┘
           │
           ▼
      ( END )
```

11. RS-232C Interface doesn't function.

```
        ( 11 )
          │
          ▼
┌─────────────────────────────────────────────────────────────────┐
│ Check transmit side.                                              │
│ Check if the switching digital signal (±5V − ±3.5V) is output to connector pin 2 during │
│ transmission.  Then check if the CTS signal of pin 5 is low level. │
│ (If not output, check M22, M24, M35, C75, C76, C77, C71, C72 and C73.) │
└─────────────────────────────────────────────────────────────────┘
          │
          ▼
┌─────────────────────────────────────────────────────────────────┐
│ Check receive side.                                              │
│ Check if a digital signal is input to M22 pin 20 (RRI terminal) during data reception. │
│ Check also to be sure that the RTSR signal of pin 4 is low level. │
│ (If not emitted, check M22, M35, M33, D9, D8 and D10.)           │
└─────────────────────────────────────────────────────────────────┘
          │
          ▼
┌──────────────────────────────────────────┐
│ Check the RS-232C select signal.          │
│ Check if PB3 port (pin 32) of M25 is low level. │
│ (If not, check M25 and M34.)              │
└──────────────────────────────────────────┘
          │
          ▼
┌──────────────────────────────────────────┐
│ Check RS-232C connector and cable.        │
└──────────────────────────────────────────┘
          │
          ▼
      (  END  )
```

12. Modem Interface doesn't function.

```
        ( 12 )
           |
           v
+---------------------------------------------------------------+
| Check transmit side.                                          |
| Check if a modulation signal is output to connector pin 5     |
| (during coupler mode) or pin 7 (during direct mode) during    |
| transmission. Then check if the receiver carrier is input to  |
| the M31 Rx Car terminal (pin 1).                              |
| (If not, check M22, M30, T4, T7, OT1 and RY2.)                |
+---------------------------------------------------------------+
           |
           v
+---------------------------------------------------------------+
| Check receive side.                                           |
| Check to be sure that the modulation signal is input to M31   |
| pin 1 (Rx Car) during data reception.                         |
| (If not, check M29, M30, OT1, T2, T3, T5, D1, D2 and RY2.     |
| If it is input, check M22 and M31.)                           |
+---------------------------------------------------------------+
           |
           v
+---------------------------------------------+
| Check the automatic dialer.                 |
| Check RY2, RY3, T7, T24, M36 and M26.       |
+---------------------------------------------+
           |
           v
    (      END      )
```

13. All functions OK?

```
        ( 13 )
           |
           v
+-----------------------------------------------------------+
| Check unit again, as described in the TROUBLESHOOTING GUIDE.|
+-----------------------------------------------------------+
```

Check List

After completing the repairs and adjustments, check all functions according to the test program below. Before beginning the test, you must initialize the RAM contents (perform a Cold Start).

1. **Buzzer and LCD Check (in BASIC mode).**

```
10 FOR I= 0 to 255
20 PRINT CHR$ (I);
30 NEXT I
40 END
```

After one beep the display clears and all printable characters are displayed.

2. **Clock Test (in BASIC mode)**

   (a) Setting the year, month, date, day, hour, minute, and seconds.
        Year, month, date setting: DATE$ = "MM/DD/YY"
        Day setting: DAY$ = "day" (Example: Sunday, sun)
        Hour, minute, second setting: TIME$ = "HH:MM:SS"

   (b) Confirmation of set data.
        Return to Main Menu and verify that the calendar data has changed to the desired settings.

3. **Keyboard Test**

   Refer to function keys in the Owner's manual and check that all functions work.

4. **Reset Function Test (Memory Protection Test)**

   (a) Warm start.
        Turn on the Computer. Press the RESET switch on the rear of the case or switch the power switch to ON, and check that initialization is made. Also check that no operator-created files have been erased.

   (b) Cold start.
        Turn the Computer ON. While pressing the (CTRL) and (PAUSE), press the RESET switch and check that all previously created files have been erased.

5. **Printer Interface Test**

   Connect a parallel printer to the Model 100. Create a file, then type some text. Press (PRINT). All the characters on the LCD should be printed out.

6. **Cassette Interface Test (in BASIC mode)**

   Type a three or four-line program and save it on tape using the CSAVE filename command. Load the program with the CLOAD filename command and verify that the program was saved accurately.

7. **RS-232C and Modem Test**

   Prepare two units to transmit and receive data — first, through the RS-232C Interface and, then, through the modem. See the Owner's manual for details.

Section 6. Illustrated Parts Breakdown

The parts list and exploded views required for maintenance, repair, and servicing TRS-80's Model 100 are provided on the pages following.

Mechanical and Assembly Parts

Ref. No.	Description	RS Part No.	Mfr's Part No.
A-1	Keyboard Assembly		AFYX1****1
A-2	P.C.B. Assembly, LCD	AX-9349	APLX1002AA
A-3	P.C.B. Assembly, Main (26-3801)	AX-9350	APLX1003AA
	(26-3802)		APLX1003BA
A-4	Case Assembly, Top	AZ-6913	AMX1****01
P-15	Plate, Model	AHC-2178	MVMX1****1
P-16	Case, Top, Silver		VB883SM001
P-17	Filter	AZ-6914	VS868AC002
A-5	Case Assembly, Bottom	AZ-6915	AMX1****02
P-18	Foot, Rubber	AF-0364	##P4157***
P-19	Battery Terminal, Front	AHC-2179	MW261LJ009
P-20	Battery Terminal, Rear	AHC-2180	MW261LJ010
P-21	Case, Bottom		VB883SB008
P-26	Buzzer Assembly	AB-7119	AYX1N***01
P-6	Cover, ROM	ADA-0386	VS667SB002
P-7	Cover, Battery	ADB-0455	VS668SB002
P-8A	Pouch	AZ-6916	AMX1****03
P-3	Plate, Name	AHC-2181	KLX1****01
P-4	Label, FCC (26-3801 USA Version Only)		KL000304XX
	(26-3802 USA Version Only)		KL000305XX
P-5	Plate, Serial Number (26-3801)		MVSX1****1
	(26-3802)		MVSX1****2
P-1	Support, Keyboard (Front)	AHC-2182	MU821LJ001
P-2	Support, Keyboard (Rear)	AHC-2183	VL821SB001
P-43	Support, Keyboard (Middle)	AHC-2233	VL122SB001
P-44	Support, Cap, Keyboard	AHC-2232	VB111RB001
P-39	Plate, Blind (Left)	AHC-2184	VS326SB003
P-40	Plate, Blind (Right)	AHC-2185	VS326SB004
P-41	Cap, RS-232C, Connector Cover	AHC-2234	VL722SB002
P-42	Cap, B.C.R., Connector Cover	AHC-2235	VE32JPB001
P-45	Plate, Shield	ART-4964	AMX1****04
S-1	Screw, Cup Head, Machine, M3X8, S-ZNCR	AHD-1865	BSP43008NZ
S-2	Screw, Pan Head, Machine, M2X4, Plastic	AHD-2612	BSPP2004NP
S-5	Screw, Pan Head, Tapping, M3X10, S-ZNCR	AHD-2619	BTPP3010BZ
S-6	Screw, Pan Head, Sems, Machine, M3X10, S-ZNCR	AHD-1867	BSPN3010NZ
S-3	Screw, Hardware Kit, Sems, Machine, M3X8, X4	AHW-2603801	NSAX110001

EXPLODED VIEW
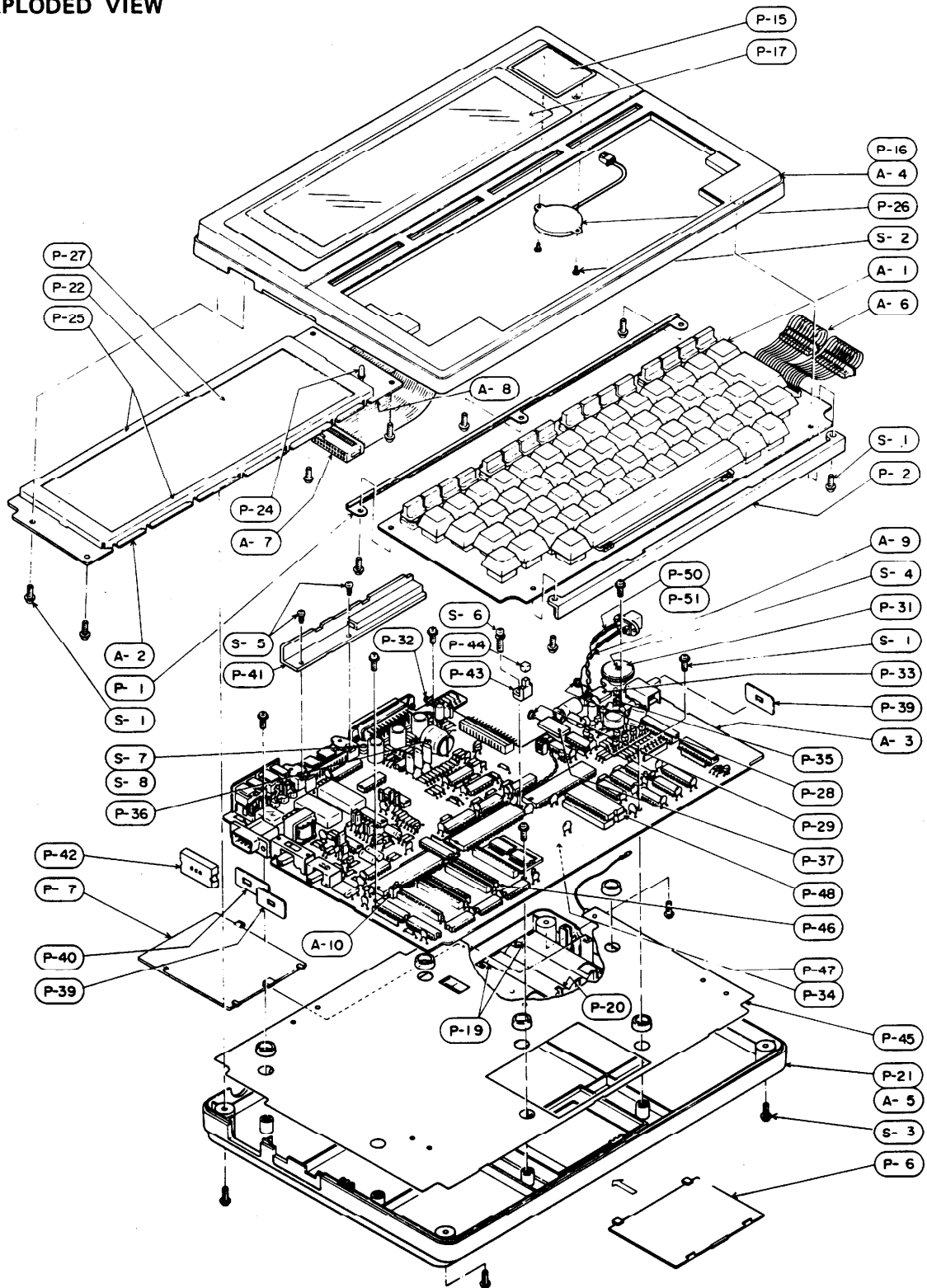
Figure 6-1 Exploded View

MEMORY POWER

ON☐☐☐☐OFF

P-4
P-5
P-3
P-18
P-21
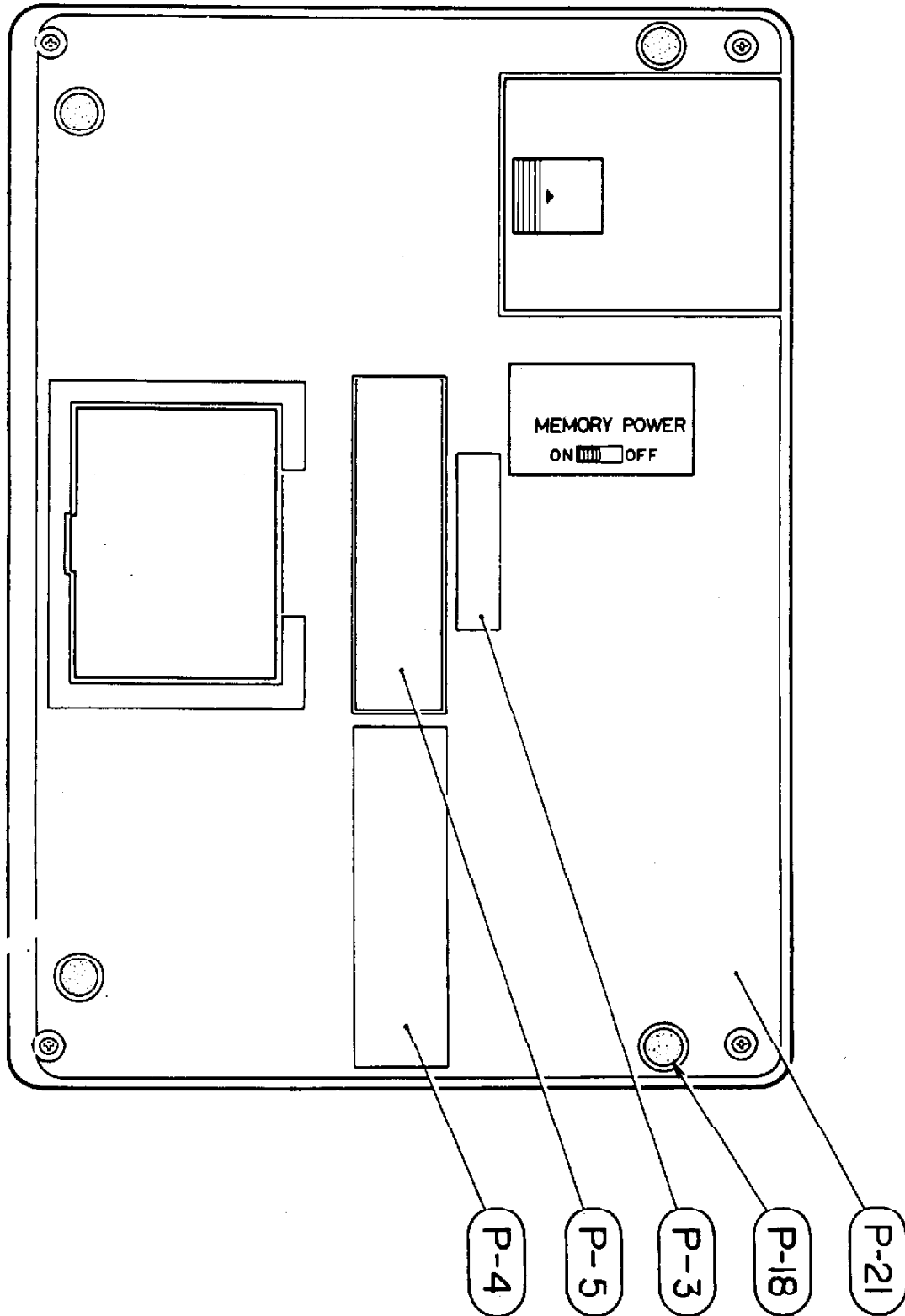
Figure 6-2 Bottom View

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Electrical Parts

The schematics and printed circuit board views (figures 6-3 thru 6-8) are shown on pages 71-75.

MAIN P.C.B ASSEMBLY

Ref. No.	Description	RS Part No.	Mfr's Part No.
C1	Capacitor, Ceramic 0.047μF, 25V, + − 10%	ACC-473KFCP	CBF1E473KM
C2			
C3			
C4	Capacitor, Ceramic 0.047μF, 25V, + − 10%	ACC-473KFCP	CBF1E473KM
C5	Capacitor, Tantalum 1μF, 10V, + − 20%	ACC-105MCTP	CSSC010MDC
C6			
C7			
C8	Capacitor, Tantalum 1μF, 10V, + − 20%	ACC-105MCTP	CSSC010MDC
C9	Capacitor, Ceramic 0.1μF, 16V, + − 20%		CBF1B104MY
C10			
C11	Capacitor, Ceramic 0.1μF, 16V, + − 20%		CBF1B104MY
C12	Capacitor, Ceramic 0.047μF, 25V, + − 10%	ACC-473KFCP	CBF1E473KM
C13			
C14			
C15			
C16	Capacitor, Ceramic 0.047μF, 25V, + − 10%	ACC-473KFCP	CBF1E473KM
C17	Capacitor, Ceramic 20pF, 50V, + − 10%	ACC-200KJCP	CCFB200KCT
C18	Capacitor, Ceramic 20pF, 50V, + − 10%	ACC-200KJCP	CCFB200KCT
C19	Capacitor, Ceramic 0.047μF, 25V, + − 10%	ACC-473KFCP	CBF1E473KM
C20	Capacitor, Ceramic 82pF, 50V, + − 10%	ACC-820KJCP	CCFB820K0T
C21			
C22			
C23			
C24			
C25			
C26			
C27	Capacitor, Ceramic 82pF, 50V, + − 10%	ACC-820KJCP	CCFB820K0T
C28	Capacitor, Ceramic 0.047μF, 25V, + − 10%	ACC-473KFCP	CBF1E473KM
C29	Capacitor, Ceramic 10pF, 50V, + − 0.5%		CCFB100DCT
C30	Capacitor, Ceramic 10pF, 50V, + − 0.5%		CCFB100DCT
C31	Capacitor, Tantalum 1μF, 10V, + − 20%	ACC-105MCTP	CSSC010MDC
C32	Capacitor, Ceramic 0.047μF, 25V, + − 10%	ACC-473KFCP	CBF1E473KM
C33			
C34			
C35	Capacitor, Ceramic 0.047μF, 25V, + − 10%	ACC-473KFCP	CBF1E473KM
C36	Capacitor, Ceramic 0.1μF, 16V, + − 20%		CBF1B104MY
C37	Capacitor, Ceramic 0.1μF, 16V, + − 20%		CBF1B104MY
C38	Capacitor, Ceramic 100pF, 50V, + − 5%		CCFB101JLT
C39	Capacitor, Ceramic 0.047μF, 25V, + 10%	ACC-473KFCP	CBF1E473KM
C40	Capacitor, Mylar 0.047μF, 50V, + − 5%	ACC-473JJMP	CQMB473JTH
C41	Capacitor, Poly Film 4700pF, 100V, + − 1%		CQPC472FEN
C42			
C43			
C44			
C45			
C46	Capacitor, Poly Film 4700pF, 100V, + − 1%		CQPC472FEN
C47	Capacitor, Ceramic 0.1μF, 16V, + − 20%		CBF1B104MY
C48	Capacitor, Ceramic 0.1μF, 16V, + − 20%		CBF1B104MY

Ref. No.	Description	RS Part No.	Mfr's Part No.
C49	Capacitor, Elec. 10μF, 16V, + −20%		CEAD100ADN
C50	Capacitor, Elec. 10μF, 16V, + −20%		CEAD100ADN
C52	Capacitor, Elec. 1μF, 50V, +75 −10%		CEAG010NLN
C53	Capacitor, Ceramic 0.1μF, 16V, + −20%		CBF1B104MY
C54	Capacitor, Elec. 10μF, 16V, + −20%		CEAD100ADN
C55	Capacitor, Elec. 10μF, 16V, + −20%		CEAD100ADN
C56	Capacitor, Ceramic 0.1μF, 16V, + −20%		CBF1B104MY
C57			
C58	Capacitor, Ceramic 0.1μF, 16V, + −20%		CBF1B104MY
C59	Capacitor, Mylar 3300pF, 50V, + −5%	ACC-332JJMP	CQMB332JTH
C60	Capacitor, Mylar 3300pF, 50V, + −5%	ACC-332JJMP	CQMB332JTH
C61	Capacitor, Mylar 4700pF, 50V, + −5%	ACC-472JJMP	CQMB472JTH
C62	Capacitor, Ceramic 10000pF, 50V, +100 −0%		CKFB103PEM
C63	Capacitor, Mylar 0.1μF, 50V, + −10%		CQMB104KTH
C64	Capacitor, Mylar 0.047μF, 50V, + −10%		CQMB473KTH
C65	Capacitor, Ceramic 0.047μF, 25V, + −10%	ACC-473KFCP	CBF1E473KM
C66			
C67	Capacitor, Ceramic 0.047μF, 25V, + −10%	ACC-473KFCP	CBF1E473KM
C69	Capacitor, Ceramic 1000pF, 50V + −10%		CKFM102KBT
C70	Capacitor, Ceramic 0.1μF, 16V, + −20%		CBF1B104MY
C71	Capacitor, Mylar 0.039μF, 50V, + −10%		CQMB393KTH
C72			
C73	Capacitor, Mylar 0.039μF, 50V, + −10%		CQMB393KTH
C74	Capacitor, Ceramic 0.047μF, 25V, + −10%	ACC-473KFCP	CBFIE473KM
C75	Capacitor, Elec. 47μF, 16V, + −20%		CEAD470NLX
C76			
C77	Capacitor, Elec. 47μF, 16V, + −20%		CEAD470NLX
C78	Capacitor, Elec. 3.3μF, 50V, + −75 −10%	ACC-335XJAP	CEVG3R3ALN
C79	Capacitor, Ceramic 0.047μF, 25V, + −10%	ACC 473KFCP	CBF1E473KM
C80	Capacitor, Ceramic 0.047μF, 25V, + −10%	ACC-473KFCP	CBF1E473KM
C81	Capacitor, Ceramic 1000pF, 50V, +80 −20%	ACC-102ZJCP	CKFB102ZFN
C82	Capacitor, Elec. 4.7μF, 25V, + −20%		CEAE4R7ADN
C83	Capacitor, Elec. 470μF, 10V, +30 −10%	ACC-477RCAP	CEAC471ACX
C84	Capacitor, Elec. 470μF, 6.3V, +30 −10%	ACC-477RBAP	CEAB471ACX
C85	Capacitor, Elec. 33μF, 10V, + −20%	ACC-336MCAP	CEAC330ADN
C86	Capacitor, Elec. 100μF, 6.3V, +75 −10%	ACC-107XBAP	CEAB101ALN
C87	Capacitor, Ceramic 0.1μF, 16V, + −20%		CBF1B104MY
C88	Capacitor, Tantalum 2.2μF, 16V, + −20%	ACC-225MDTP	CSSD2R2MDC
C89	Capacitor, Tantalum 2.2μF, 16V, + −20%	ACC-225MDTP	CSSD2R2MDC
C90	Capacitor, Elec. 1μF, 50V, + −20%		CEAG010ADN
C91	Capacitor, Ceramic 0.047μF, 25V, + −10%	ACC-473KFCP	CBF1E473KM
C92	Capacitor. Elec. 0.47μF. 50V. +75 −10%	ACC-474XJAP	CEAGR47ALN
C94	Capacitor, Ceramic 8200pF, 50V, + −10%	ACC-822KJCP	CKFB822KBT
C97	Capacitor, Ceramic 1000pF, 50V, + −10%		CKFB102KBT
C98	Capacitor, Ceramic 1000pF, 50V, + −10%		CKFB102KBT
C99	Capacitor, Ceramic 0.047μF, 25V, + −10%	ACC-473KFCP	CBF1E473KM
C100	Capacitor, Ceramic 2200pF, 50V, + −10%		CKFB222KBT
C101	Capacitor, Tantalum 1μF, 10V, + −20%	ACC-105MCTP	CSSC010MDC
C102	Capacitor, Ceramic 100pF, 50V, + −10%		CCFB101K0T
C103	Capacitor, Elec. 220μF, 10V, +30 −10%	ACC-227RCAP	CEAC221ACX
C104	Capacitor, Ceramic 10000pF, 50V, +100 −0%		CKFB103PEM
C105	Capacitor, Tantalum 0.15μF, 16V, + −20%	ACC-154MDTP	CSSDR15MDC
C106	Capacitor, Tantalum 0.15μF, 16V, + −20%	ACC-154MDTP	CSSDR15MDC
C107	Capacitor, Ceramic 270pF, 50V, + −10%	ACC-271KJCP	CCFB271K0T

Ref. No.	Description	RS Part No.	Mfr's Part No.
C108	Capacitor, Mylar 5600pF, 50V, + − 10%	ACC-562KJMP	CQMB562KTH
C109	Capacitor, Ceramic 68pF, 50V, + − 10%		CCFB680K0T
C110	Capacitor, Ceramic 1000pF, 50V, + − 10%		CKFB102KBT
C111	Capacitor, Ceramic 3300pF, 50V, + − 10%		CBF1H332KT
CN1	Jack, Junction, Keyboard 5268-10A	AJ-7343	YJF10S050Z
CN2	Jack, Junction, BCR CP-P26-09-30-134	AJ-7342	YJF09S045Z
CN3	Jack, Junction, CMT TCS4480-01-1011	AJ-7340	YJF08S033Z
CN4	Jack, Junction, Modem TCS4490-01-1111	AJ-7341	YJF08S034Z
CN5	Jack, Junction, Printer FRC2-C26-L13 ON	AJ-7345	YJF26S010Z
CN6	Jack, Junction, RS-232C	AJ-7344	YJF25S012Z
CN7	Jack, Junction, LCD HU-30P-2G-L13	AJ-7346	YJF30S006Z
CN8	Jack, Junction, LED Line	AJ-7322	YJF02S041Z
CN9	Jack, HECO342-01-010	AJ-7338	YJB03S001Z
D1	Diode, Silicon 1S2076		QDSS2076#B
D2	Diode, Silicon 1S2076		QDSS2076#B
D4	Diode, Silicon, Zener, NEC RD4.3 EL3	ADX-1860	QDZ4R3EL3A
D5	Diode, Silicon 1S2076		QDSS2076#B
D6			
D7			
D8			
D9			
D10			
D11			
D12	Diode, Silicon 1S2076		QDSS2076#B
D13	Diode, Silicon ERA81-004	ADX-1859	QDS81004XZ
D14	Diode, Silicon, Zener NEC RD5.1 EL1	ADX-1861	QDZ5R1EL1A
D15	Diode, Silicon 1S2076		QDSS2076#B
D16			
D17	Diode, Silicon 1S2076		QDSS2076#B
D18	Surge Absorber ERZ-C10DK361	ADX-1864	QNHDK361AN
D20	Diode, Silicon 1S2076		QDSS2076#B
D21			
D22	Diode, Silicon 1S2076		QDSS2076#B
D23	Diode, Silicon ERA81-004	ADX-1859	QDS81004XZ
D24	Surge Absorber ERZ-C10K220 250A	ADX-1863	QNDDK220AN
D27	Surge Absorber SNR-7D18L	ADX-1862	QNB7D18LAD
D28	Diode, Silicon 1S2076		QDSS2076#B
D29	Diode, Silicon 1S2076		QDSS2076#B
M1	IC, Hi-Speed C-MOS, or Gate, TC40H373P	AMX-5820	QQ040373AT
M2	IC, Hi-Speed C-MOS, Buffer, TC40H245P	AMX-5818	QQ040245AT
M3	IC, Hi-Speed C-MOS, Decoder, TC40H138P	AMX-5813	QQ040138AT
M4	IC, Hi-Speed C-MOS, Decoder, TC40H138P	AMX-5813	QQ040138AT
M5	IC, Hi-Speed C-MOS, Decoder, TC40H139P	AMX-5814	QQ040139AT
*M6	Assembly, RAM Package IC TC5518BF X 4	AMX-5799	QQHX1001A6
*M7	or HM6117LFP-4 X 4		QQHX1002A6
*M8			
*M9			
M12	IC, C-MOS, Masked ROM, LH535618	AMX-5821	QQ05356183

Ref. No.	Description	RS Part No.	Mfr's Part No.
M13	IC, Hi-Speed C-MOS, or Gate, TC40H032P	AMX-5812	QQ040032AT
M14	IC, Hi-Speed C-MOS, Flip Flop, TC40H175P	AMX-5816	QQ040175AT
M15	IC, Hi-Speed C-MOS, Buffer, TC40H244P	AMX-5817	QQ040244AT
M16	IC, Hi-Speed C-MOS, Decoder, TC40H138P	AMX-5813	QQ040138AT
M17	IC, Hi-Speed C-MOS, NAND Gate, TC40H000P	AMX-5810	QQ040000AT
M18	IC, C-MOS, Timer, D1990AC	AMX-5801	QQ001990BA
M19	IC, C-MOS, CPU, MSM80C85ARS	AMX-5806	QQ008085A5
M20	IC, Hi-Speed C-MOS, Buffer, TC40H367P	AMX-5819	QQ040367AT
M21	IC, Hi-Speed C-MOS, Buffer, TC40H244P	AMX-5817	QQ040244AT
M22	IC, C-MOS, UART, D3-6402-9	AMX-5805	QQ006402AZ
M23	IC, Hi-Speed C-MOS, Buffer, TC40H244P	AMX-5817	QQ040244AT
M24	IC, Hi-Speed C-MOS, or Gate, TC40H032P	AMX-5812	QQ040032AT
M25	IC, C-MOS, PI/O, MSM81C55RS	AMX-5807	QQ008155A5
M26	IC, Hi-Speed C-MOS, NOR Gate, TC40H002P	AMX-5811	QQ040002AT
M27	IC, C-MOS, NAND Gate, MN4011B or	AMX-5802	QQ004011AN
M27	IC, C-MOS, NAND Gate, D4011C		QQ004011AA
M28	IC, C-MOS, D-Flip Flop, MN4013B or	AMX-5804	QQ004013AN
M28	IC, C-MOS, D-Flip Flop, D4013C		QQ004013AA
M29	IC, Bipolar, OP AMP, TL064CN	AMX-5800	QQM00064AU
M30	IC, Bipolar, OP AMP, TL064CN	AMX-5800	QQM00064AU
M31	IC, C-MOS, Modem, MC14412VP	AMX-5808	QQ014412AM
M32	IC, Hi-Speed C-MOS. Buffer. TC40H244P	AMX-5817	QQ040244AT
M33	IC, Hi-Speed C-MOS, Selector, TC40H157P	AMX-5815	QQ040157AT
M34	IC, C-MOS, Schmitt Trigger, HD14584BP	AMX-5809	QQ014584AB
M35	IC, C-MOS, Schmitt Trigger, HD14584BP	AMX-5809	QQ014584AB
M36	IC, C-MOS, D-Flip Flop, MN4013B or	AMX-5804	QQ004013AN
M36.	IC, C-MOS, D-Flip Flop, D4013C		QQ004013AA
**P-38	IC, C-MOS, RAM, TC5518BF-25 or	AMX-5839	QQ005518AT
**P-38	IC, C-MOS, RAM, HM6117LFP-4		QQ006117BB

* 26-3801 is installed on M9.
* 26-3802 is installed on M9, M8 and M7.
** P-38 is mounted on the RAM package IC.

Ref. No.	Description	RS Part No.	Mfr's Part No.
MR1	Resistor Array, 100K X 8 1/8W, + −20%		RAB104M08X
MR2	Resistor Array, 100K X 8 1/8W, + −20%		RAB104M08X
MR3	Resistor Array, 33K X 8 1/8W, + −20%		RAB333M08X
MR4	Resistor Array, 33K X 8 1/8W, + −20%		RAB333M08X
MR5	Resistor Array, 100K X 8 1/8W, + −20%		RAB104M08X
MR6			
MR7	Resistor Array, 100K X 8 1/8W, + −20%		RAB104M08X

Ref. No.	Description	RS Part No.	Mfr's Part No.
OT1	Transformer, Driver E6732B AC1000V	ATB-0472	TDZ19A002K
OT2	Transformer, Converter TN22A	ATB-0471	TC12RZ001B

Ref. No.	Description	RS Part No.	Mfr's Part No.
R1	Res. Carbon 1K Ohm, 1/4W, + −5%		RD25PJ102X
R2	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R3			
R4			
R5			
R6			
R7	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X

Ref. No.	Description	RS Part No.	Mfr's Part No.
R8	Res. Carbon 1K Ohm, 1/4W, + −5%		RD25PJ102X
R9			
R10			
R11			
R12	Res. Carbon 1K Ohm. 1/4W. + −5%		RD25PJ102X
R13	Res. Metal Film 806 Ohm, 1/4W, + −1%	AN-0577BEC	RQBPF8060X
R14	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R15	Res. Metal Film 33.2K Ohm, 1/4W, + −1%	AN-0622BEC	RQBPF3322X
R16	Res. Metal Film 2.05K Ohm, 1/4W, + −1%	AN-0716BEC	RQBPF2051X
R17	Res. Metal Film 73.2K Ohm, 1/4W, + −1%	AN-0612BEC	RQBPF7322X
R18	Res. Metal Film 590K Ohm, 1/4W, + −1%	AN-0615BEC	RQBPF5903X
R19	Res. Carbon 15K Ohm, 1/4W, + −5%		RD25PJ153X
R20	Res. Carbon 470K, 1/4W, + −5%		RD25PJ474X
R21	Res. Carbon 620 Ohm, 1/4W, + −5%		RD25PJ621X
R22	Res. Carbon 390 Ohm, 1/4W, + −5%		RD25PJ391X
R23	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R24	Res. Metal Film 665 Ohm, 1/4W, + −1%		RQBPF6650X
R25	Res. Metal Film 1.5K Ohm, 1/4W, + −1%	AN-0206BEC	RQBPF1501X
R26	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R27	Res. Metal Film 1.30K Ohm, 1/4W, + −1%		RQBPF1301X
R28	Res. Metal Film 3.3K Ohm, 1/4W, + −1%	AN-0230BEC	RQBPF3301X
R29	Res. Metal Film 280K Ohm, 1/4W, + −1%	AN-0672BEC	RQBPF2803X
R30	Res. Metal Film 422K Ohm, 1/4W, + −1%	AN-0419BEC	RQBPF4223X
R31	Res. Carbon 2.2K Ohm, 1/4W, + −5%		RD25PJ222X
R32	Res. Carbon 22 Ohm, 1/4W, + −5%		RD25PJ220X
R33	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R34	Res. Carbon 1K Ohm, 1/4W, + −5%		RD25PJ102X
R35	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R36	Res. Carbon 680 Ohm, 1/4W, + −5%		RD25PJ681X
R37	Res. Carbon 180K Ohm, 1/4W, + −5%		RD25PJ184X
R38	Res. Metal Film 52.3K Ohm, 1/4W, + −1%	AN-0613BEC	RQBPF5232X
R39	Res. Carbon 1K Ohm, 1/4W, + −5%		RD25PJ102X
R40	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R41	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R42	Res. Metal Film 2.3K Ohm, 1/4W, + −1%		RQBPF2301X
R43	Res. Metal Film 10K Ohm, 1/4W, + −1%		RQBPF1002X
R44	Res. Metal Film 242K Ohm, 1/4W, + −1%		RQBPF2423X
R45	Res. Metal Film 7.97K Ohm. 1/4W. + −1%		ROBPF7971X
R46	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R47	Res. Carbon 15M Ohm, 1/4W, + −5%		RD25TJ156X
R48	Res. Carbon 68K Ohm, 1/4W, + −5%		RD25PJ683X
R49	Res. Carbon 3.3K Ohm, 1/4W, + −5%		RD25PJ332X
R50	Res. Carbon 3.3K Ohm, 1/4W, + −5%		RD25PJ332X
R51	Res. Carbon 2.2K Ohm, 1/4W, + −5%		RD25PJ222X
R52	Res. Carbon 1K Ohm, 1/4W, + −5%		RD25PJ102X
R53	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R54	Res. Carbon 12K Ohm, 1/4W, + −5%		RD25PJ123X
R55	Res. Carbon 3.3K Ohm. 1/4W. + −5%		RD25PJ332X
R56	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R57	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R58			
R59			
R60			
R61			
R62	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X

Ref. No.	Description	RS Part No.	Mfr's Part No.
R63	Res. Carbon 620 Ohm, 1/4W, + −5%		RD25PJ621X
R64	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R65			
R66			
R67			
R68			
R70			
R71			
R72			
R73			
R74	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R75	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R76	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R77	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R78	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R79	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R80	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R81	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R82	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R83	Res. Carbon 22K Ohm, 1/4W, + −5%		RD25PJ223X
R84	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R85	Res. Carbon 10K Ohm, 1/4W, + 5%		RD25PJ103X
R86	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R87	Res. Carbon 6.2K Ohm, 1/4W, + −5%		RD25PJ622X
R88			
R89	Res. Carbon 6.2K Ohm, 1/4W, + −5%		RD25PJ622X
R90	Res. Carbon 15K Ohm, 1/4W, + −5%		RD25PJ153X
R91	Res. Carbon 5.6K Ohm, 1/4W, + −5%		RD25PJ562X
R92	Res. Carbon 18K Ohm, 1/4W, + −5%		RD25PJ183X
R93	Res. Carbon 68K Ohm, 1/4W, + −5%		RD25PJ683X
R94	Res. Carbon 5.6K Ohm, 1/4W, + −5%		RD25PJ562X
R95	Res. Carbon 100 Ohms, 1/4W, + −5%		RD25PJ101X
R96	Res. Carbon 18K Ohm, 1/4W, + −5%		RD25PJ183X
R97	Res. Carbon 180 Ohm, 1/4W, + −5%		RD25PJ181X
R98	Res. Carbon 18K Ohm, 1/4W, + −5%		RD25PJ183X
R99	Res. Carbon 5.6K Ohm, 1/4W, + −5%		RD25PJ562X
R101	Res. Carbon 1.8K Ohm, 1/4W, + −5%		RD25PJ182X
R102	Res. Carbon 82K Ohm, 1/4W, + −5%		RD25PJ823X
R103	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R104	Res. Carbon 56K Ohm, 1/4W, + −5%		RD25PJ563X
R105	Res. Metal Film 2.7K Ohm, 1/4W, + −1%	AN-0224BEE	RQBPF2701X
R106	Res. Carbon 150K Ohm, 1/4W, + −5%		RD25PJ154X
R107	Res. Carbon 47K Ohm, 1/4W, + −5%		RD25PJ473X
R108	Res. Metal Film 22.6K Ohm, 1/4W, + −1%		RQBPF2262X
R109	Res. Carbon 56K Ohm, 1/4W, + −5%		RD25PJ563X
R110	Res. Carbon 150K Ohm, 1/4W, + −5%		RD25PJ154X
R111	Res. Carbon 150K Ohm, 1/4W, + −5%		RD25PJ154X
R112	Res. Carbon 1.8K Ohm, 1/4W, + −5%		RD25PJ182X
R113	Res. Carbon 3.3K Ohm, 1/4W, + −5%		RD25PJ332X
R114	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R115	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R116	Res. Metal Film 150K Ohm, 1/4W, + −1%		RQBPF1503X
R118	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R119	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X

Ref. No.	Description	RS Part No.	Mfr's Part No.
R120	Res. Carbon 82K Ohm, 1/4W, + −5%		RD25PJ823X
R121	Res. Carbon 820 Ohm, 1/4W, + −5%		RD25PJ821X
R122	Res. Carbon 470 Ohm, 1/4W, + −5%		RD25PJ471X
R123	Res. Carbon 1.8K Ohm, 1/4W, + −5%		RD25PJ182X
R124	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R125	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R126	Res. Carbon 270 Ohm, 1/4W, + −5%		RD25PJ271X
R127	Res. Carbon 22K Ohm, 1/4W, + −5%		RD25PJ223X
R128	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R131	Res. Carbon 1K Ohm, 1/4W, + −5%		RD25PJ102X
R132	Res. Carbon 150K Ohm, 1/4W, + −5%		RD25PJ154X
R134	Res. Carbon 3.3K Ohm, 1/4W, + −5%		RD25PJ332X
R135	Res. Carbon 68K Ohm, 1/4W, + −5%		RD25PJ683X
R136	Res. Carbon 68K Ohm, 1/4W, + −5%		RD25PJ683X
R137	Res. Carbon 100K Ohm, 1/4W, ⏐ 5%		RD25PJ104X
R138			
R139	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R140	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R141	Res. Carbon 1Meg Ohm, 1/4W, + −5%		RD25PJ105X
R142	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R144	Res. Carbon 15K Ohm, 1/4W, + −5%		RD25PJ153X
R145	Res. Carbon 15K Ohm, 1/4W, + −5%		RD25PJ153X
R146	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R149	Res. Carbon 56K Ohm, 1/4W, + −5%		RD25PJ563X
R150	Res. Carbon 470 Ohm, 1/4W, + −5%		RD25PJ471X
R151	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R152	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R153	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R154	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R156	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R157	Res. Carbon 33K Ohm, 1/4W, + −5%		RD25PJ333X
R158	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R159	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R160	Res. Carbon 100K Ohm, 1/4W, + −5%		RD25PJ104X
R161	Res. Carbon 10K Ohm, 1/4W, + −5%		RD25PJ103X
R162	Res. Carbon 100 Ohm, 1/4W, + −5%	AN-0132EBC	RD18TJ101X
R170	Res. Carbon 150K Ohm, 1/4W, + −5%		RD25PJ154X
RY1	Relay FBR211CD005-M	AR-8160	ZRA265101Z
RY2	Relay FRL-764D05. 1AS-T	AR-8159	ZRA164102Z
RY3	Relay FRL-764D05, 1BS-T Modem	AR-8158	ZRA164101Z
SW1	Switch, Slide Shorting Knob 9MM, PWR, ANS	AS-2843	SS020259ZA
SW2	Switch, Slide SSB34204, Modem	AS-2845	SS040213ZA
SW3	Switch, Slide SLB-22B9-03 Knob 3MM, BKUP	AS-2844	SS020260ZL
SW4	Switch, Push SPJ312U w/o Knob, Reset	AS-7573	SP01ABA06A
SW5	Switch, Slide Shorting Knob 9MM, PWR, ANS	AS-2843	SS020259ZA
T1	Xsistor 2SA1115 No Rank PC300MW, FT200MH		QTA1115XAE
T2	Xsistor 2SC2603 No Rank PC300MW, FT200MH	AA-2SC2603	QTC2603XAE
T3			

Ref. No.	Description	RS Part No.	Mfr's Part No.
T4			
T5			
T6			
T7			
T8			
T9			
T10			
T11	Xsistor 2SC2603 No Rank PC300MW, FT200MH	AA-2SC2603	QTC2603XAE
T13	Xsistor 2SC2603 E-Rank PC300MW, FT200MHz		QTC2603XCE
T14			
T15			
T16			
T17	Xsistor 2SC2603 E-Rank PC300MW, FT200MHz		QTC2603XCE
T18	Xsistor 2SC2603 No Rank PC300MW, FT200MH	AA-2SC2603	QTC2603XAE
T19	Xsistor 2SA1115 No Rank PC300MW, FT200MH		QTA1115XAE
T20	Xsistor 2SC2603 No Rank PC300MW, FT200MH	AA-2SC2603	QTC2603XAE
T21	Xsistor 2SC1384 S-Rank PC750MW, FT200MHz		QTC1384XHN
T22	Xsistor 2SC2603 E-Rank PC300MW, FT200MHz		QTC2603XCE
T23	Xsistor 2SC2603 No Rank PC300MW, FT200MH	AA-2SC2603	QTC2603XAE
T24			
T25			
T27	Xsistor 2SC2603 No Rank PC300MW, FT200MH	AA-2SC2603	QTC2603XAE
T28	Xsistor 2SA1115 No Rank PC300MW, FT200MH		QTA1115XAE
TH1	Thermistor 10K Ohm, + −5% TD5-C310D1	AT-1235	QHQ5C31HZP
TH2	Thermistor 10K Ohm, + −5% TD5-C310D1	AT-1235	QHQ5C31HZP
VR1	Var. Resistor 50K, B LCD Contrast		RV9A503B01
VR2	Var. Resistor Semi-Fixed 50K, B Modem LE		RPSNB50303
X1	Xtal Oscillator 32.768kHz + −20PPM	AMX-1011	XTR1A1001%
X2	Xtal Oscillator 4.9152MHz	AMX 1010	XBR1A1003X
X3	Xtal Oscillator HC43, U 1MHz	AMX-1009	XAZ1C2001X

MISCELLANEOUS

Ref. No.	Description	RS Part No.	Mfr's Part No.
A-9	Connector, Main PCB Assy	AJ-7323	ACCNA02GEA
A-10	Connector, Main PCB Assy	AJ-7325	ACCNA05GEA
P-28	Battery Terminal, Negative	AHC-2156	MW361SN001
P-29	Battery Terminal, Positive	AHC-2157	MW361SN003
P-31	Knob, Volume	AK-5264	VF122SB001
P-32	Knob, Reset	AK-5265	VK121SD004
P-33	Support, Battery, Minus	AHC-2177	VS118SB001
P-34	Socket, I.C. ICA40-STG	AJ-7350	YSC40S002Z
P-35	Terminal, Shield Plate	AJ-7351	YZC1150001
P-36	Battery Ni-Cad 3-51FT	ACS-0100	ZBN036102Y
P-37	Support, Battery, Positive		VS218SB002
P-46	Socket, I.C. SBA-STG	AJ-7347	YSC14S002Z
P-47	Socket, I.C. A-8878A-28S-1H	AJ-7348	YSC28S002Z
P-48	Socket, I.C. DICF-28CS	AJ-7349	YSC28S005Z
P-50	Coil, Choke 10μH, 500mMA, Axial	ACA-8286	LF100KE04Y

Ref. No.	Description	RS Part No.	Mfr's Part No.
P-51	Ferrite Bead		YFRL000002
S-4	Screw, Pan Head, Machine, M1.7X3, S-Black	AHD-2593	BSP21703NB
S-7	Screw, Pan Head, Sems, Machine, M3X8, S-ZNCR	AHD-2594	BSPC3008NZ
S-8	Nut, M3 Z-ZNCR Thin Type	AHD-7284	BNHCL30NSZ

LCD P.C.B. ASSEMBLY

Ref. No.	Description	RS Part No.	Mfr's Part No.
LC1	Capacitor, Cera Chip 0.1μF, 25V, +80−20%	ACD-104ZFCX	CFKC104ZF%
LC2			
LC3			
LC4	Capacitor, Cera Chip 0.1μF, 25V, +80−20%	ACD-104ZFCX	CFKC104ZF%
LC5	Capacitor, Cera Chip 18pF, 25V, +−10%	ACD-180KFCX	CFKC180KC%
LC6	Capacitor, Cera Chip 0.1μF, 25V, +80−20%	ACD-104ZFCX	CFKC104ZF%
LC7			
LC8			
LC9			
LC10	Capacitor, Cera Chip 0.1μF, 25V, +80−20%	ACD-104ZFCX	CFKC104ZF%
LC11	Capacitor, Cera Chip 1000pF, 25V, +80−20%	ACD-102ZFCX	CFKC102ZF%
LC12			
LC13			
LC14			
LC15			
LC16			
LC17			
LC18			
LC19			
LC20	Capacitor, Cera Chip 1000pF, 25V, +80−20%	ACD-102ZFCX	CFKC102ZF%
LC21	Capacitor, Cera Chip 220pF, 25V, +80−20%	ACD-221ZFCX	CFKC221ZF%
LC22			
LC23			
LC24			
LC25	Capacitor, Cera Chip 220pF, 25V, +80−20%	ACD-221ZFCX	CFKC221ZF%
LC26	Capacitor, Ceramic 0.047μF, 25V, +−10%		CBD1E473KM
LCN6	Jack, Junction Buzzer B2B-XH-A	AJ-7322	YJF02S041Z
LM1	IC, C-MOS, Driver, HD44102CH	AMX-5797	QQ044102BB
LM2			
LM3			
LM4			
LM5			
LM6			
LM7			
LM8			
LM9			
LM10	IC, C-MOS, Driver, HD44102CH	AMX-5797	QQ044102BB
LM11	IC, C-MOS, Driver, HD44103BLD	AMX-5798	QQ044103BB
LM12	IC, C-MOS, Driver, HD44103BLD	AMX-5798	QQ044103BB
LM13	IC, Bipolar, OP AMP, HA17902P	AMX-5796	QQM17902PB

Ref. No.	Description	RS Part No.	Mfr's Part No.
LR1	Resistor, Chip 10K Ohm, 1/8W, + − 2%		RJ8AMG103%
LR2	Resistor, Chip 10K Ohm, 1/8W, + − 2%		RJ8AMG103%
LR3	Resistor, Chip 26.5K Ohm, 1/8W, + − 2%		RJ8AMGA52%
LR4	Resistor, Chip 10K Ohm, 1/8W, + − 2%		RJ8AMG103%
LR5	Resistor, Chip 10K Ohm, 1/8W, + − 2%		RJ8AMG103%
LR6	Resistor, Chip 100K Ohm, 1/8W, + − 5%		RJ8AMJ104%
LR7			
LR8			
LR9			
LR10	Resistor, Chip 100K Ohm, 1/8W, + − 5%		RJ8AMJ104%
LR11	Resistor, Chip 18 Ohm, 1/8W, + − 5%		RJ8AMJ180%
LR12	Resistor, Chip 150 Ohm, 1/8W, + − 5%		RJ8AMJ151%
LR13			
LR14			
LR15			
LR16	Resistor, Chip 150 Ohm, 1/8W, + − 5%		RJ8AMJ151%

MISCELLANEOUS

Ref. No.	Description	RS Part No.	Mfr's Part No.
A-7	Cord Assy – LCD Connector	AW-3058	ACCN812GEA
A-8	Connector Assy – LCD PCB	AJ-7324	ACCNA03GEA
P-22	Holder – LCD	AHC-2154	MB861SF001
P-24	L.E.D. SLP-135B	AL-1458	QL1SP135BC
P-25	Connector, LCD SG Type	AJ-7321	VQ811RX1001
P-27	L.C.D. LR202 C	AL-1459	ZXLR202CXB

KEYBOARD ASSEMBLY

Ref. No.	Description	RS Part No.	Mfr's Part No.
P-12	Switch, Key – Tact	AS-7570	SK0101X10A
P-13	Switch, Key – Push	AS-7571	SK0111X04A
P-14	Switch, Key – Lock Type	AS-7572	SK0111X05A

MISCELLANEOUS

Ref. No.	Description	RS Part No.	Mfr's Part No.
A-6	Cord Assy – Key Board Connector	AW-3057	ACCN870GEA
P-10	Guide – Space Key	AHC-2153	MX722LJ001
P-9	Guide – Enter Key	AHC-2152	MX422LJ001

KEYTOPS

Ref. No.	Description	RS Part No.	Mfr's Part No.
P-100	Keytop – Tact	AK-5205	VK121SB003
P-101	Keytop – 1	AK-5206	VK122SB004
P-102	Keytop – 2	AK-5207	VK122SB005
P-103	Keytop – 3	AK-5208	VK122SB006
P-104	Keytop – 4	AK-5209	VK122SB007
P-105	Keytop – 5	AK-5210	VK122SB008
P-106	Keytop – 6	AK-5211	VK122SB009
P-107	Keytop – 7	AK-5212	VK122SB010
P-108	Keytop – 8	AK-5213	VK122SB011
P-109	Keytop – 9	AK-5214	VK122SB012
P-110	Keytop – 0	AK-5215	VK122SB013
P-111	Keytop – A	AK-5216	VK122SB014

Ref. No.	Description	RS Part No.	Mfr's Part No.
P-112	Keytop – B	AK-5217	VK122SB015
P-113	Keytop – C	AK-5218	VK122SB016
P-114	Keytop – D	AK-5219	VK122SB017
P-115	Keytop – E	AK-5220	VK122SB018
P-116	Keytop – F	AK-5221	VK122SB019
P-117	Keytop – G	AK-5222	VK122SB020
P-118	Keytop – H	AK-5223	VK122SB021
P-119	Keytop – I	AK-5224	VK122SB022
P-120	Keytop – J	AK-5225	VK122SB023
P-121	Keytop – K	AK-5226	VK122SB024
P-122	Keytop – L	AK-5227	VK122SB025
P-123	Keytop – M	AK-5228	VK122SB026
P-124	Keytop – N	AK-5229	VK122SB027
P-125	Keytop – O		VK122SB028
P-126	Keytop P	AK 5231	VK122SB029
P-127	Keytop – Q	AK-5232	VK122SB030
P-128	Keytop – R	AK-5233	VK122SB031
P-129	Keytop – S	AK-5234	VK122SB032
P-130	Keytop – T	AK-5235	VK122SB033
P-131	Keytop – U	AK-5236	VK122SB034
P-132	Keytop – V	AK-5237	VK122SB035
P-133	Keytop – W	AK-5238	VK122SB036
P-134	Keytop – X	AK-5239	VK122SB037
P-135	Keytop – Y	AK-5240	VK122SB038
P-136	Keytop – Z	AK-5241	VK122SB039
P-200	Keytop – ESC	AK-5242	VK122SB040
P-201	Keytop – Minus	AK-5243	VK122SB041
P-202	Keytop – Equal	AK-5244	VK122SB042
P-203	Keytop – DEL	AK-5245	VK122SB043
P-204	Keytop – Bracket	AK-5246	VK122SB044
P-205	Keytop – ;	AK-5247	VK122SB045
P-206	Keytop – '	AK-5248	VK122SB046
P-207	Keytop – CAPS LOCK	AK-5249	VK122SB047
P-208	Keytop – Comma	AK-5250	VK122SB048
P-209	Keytop – Period	AK-5251	VK122SB049
P-210	Keytop – /	AK-5252	VK122SB050
P-211	Keytop – Grph	AK-5253	VK122SB051
P-212	Keytop – CODE	AK-5254	VK122SB052
P-213	Keytop – NUM	AK-5255	VK122SB053
P-214	Keytop – Tab	AK-5256	VK132SB006
P-215	Keytop – CTRL	AK-5257	VK132SB007
P-216	Keytop – SHIFT	AK-5259	VK132SB008
P-217	Keytop – ENTER	AK-5260	VK142SB003
P-218	Keytop – Space	AK-5261	VK172SB002
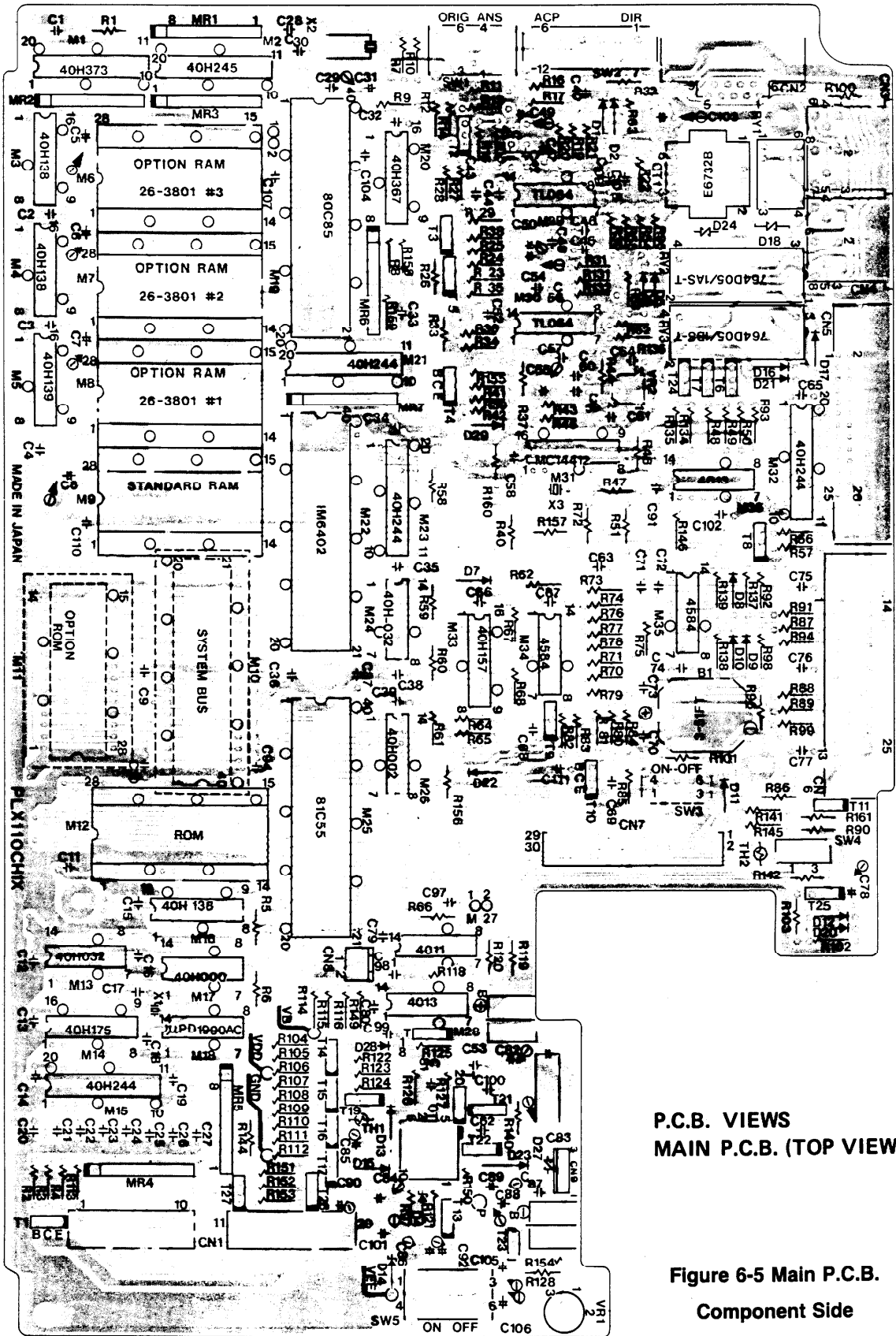
P.C.B. VIEWS
MAIN P.C.B. (TOP VIEW)

Figure 6-5 Main P.C.B.

Component Side

73
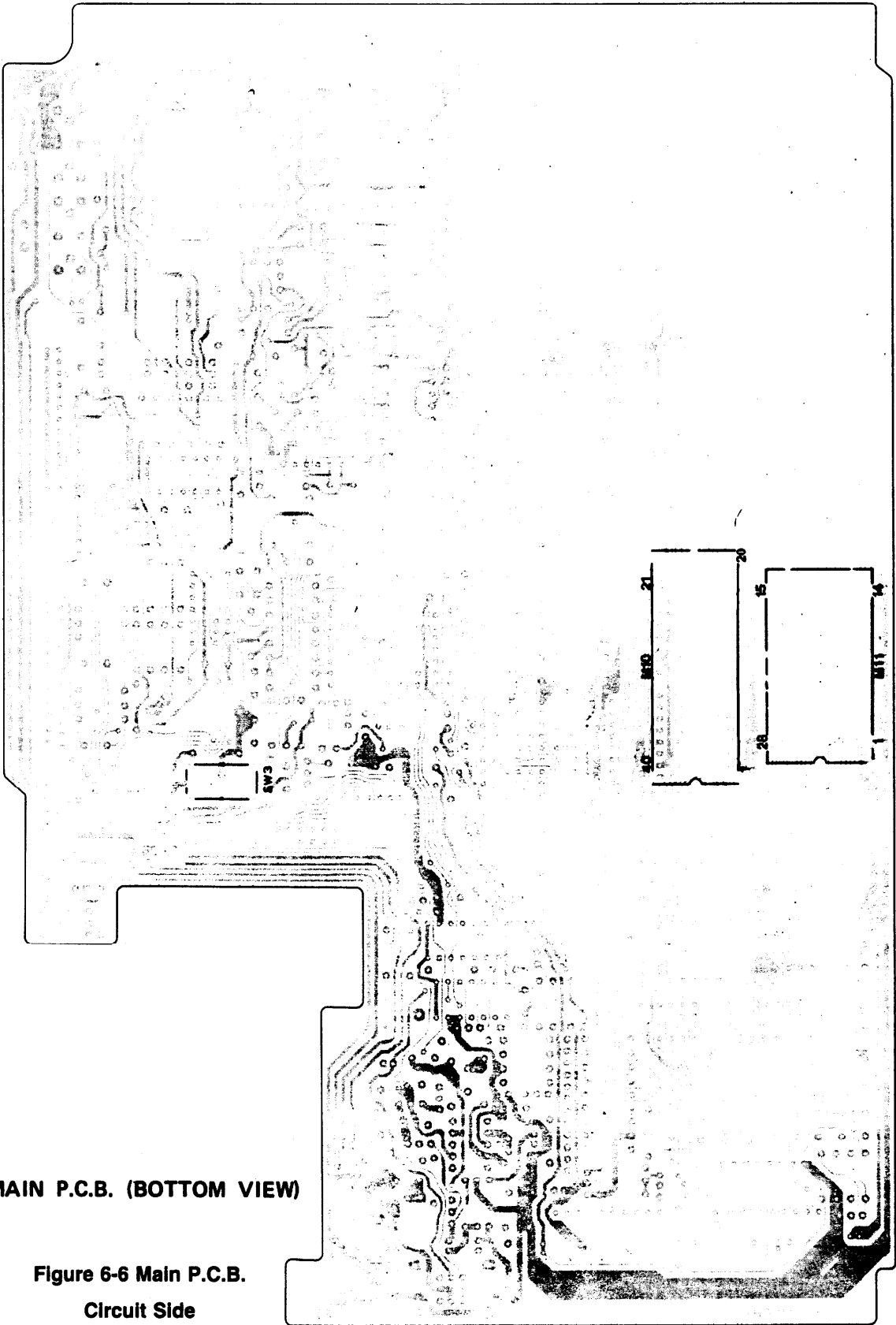
MAIN P.C.B. (BOTTOM VIEW)

Figure 6-6 Main P.C.B.
Circuit Side

LCD P.C.B. VIEWS

(TOP VIEW)
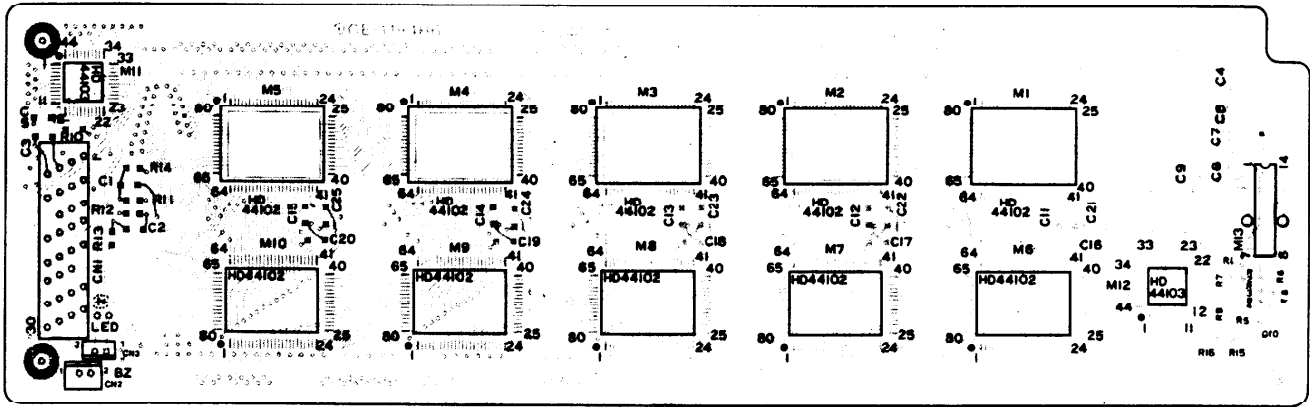
Figure 6-7 LCD P.C.B. — Component Side

(BOTTOM VIEW)
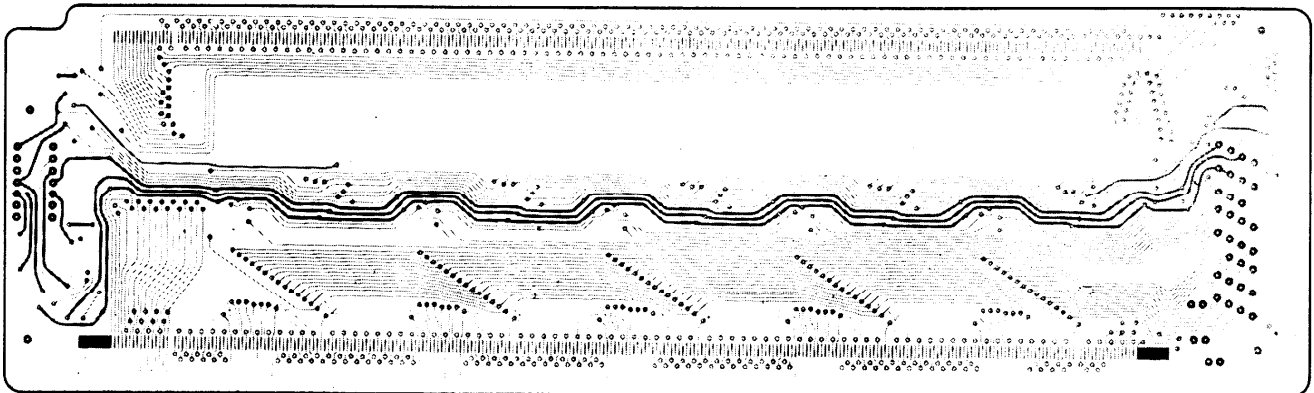
Figure 6-8 LCD P.C.B. — Circuit Side

Section 7. Optional RAM and ROM ICs

Following is the information you will need for installing the optional RAMs and ROM in the Model 100.

To install optional RAM ICs:

1. Open the top and bottom case of the Model 100. Refer to **Section 2, Disassembly/Reassembly**.

2. Find the three IC sockets marked "Optional RAM 26-3801 #1, 2, and 3." Be sure that the RAM IC pins are correctly aligned with the sockets.

3. Insert the three optional RAM ICs into the sockets.

4. Replace the cases.

To install optional ROM IC:

1. Using a flat object, such as a coin, pry open the ROM cover on the bottom case.

2. Insert the optional ROM IC into the socket with the plastic housing. Be sure to align the pin numbers in the four corners of the socket (marked 1. 14. 15. and 28) with the ROM IC.

3. Place the ROM cover over the optional ROM, snapping it shut.
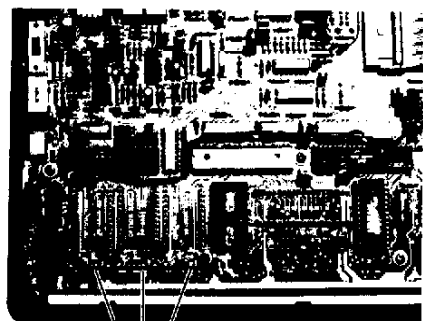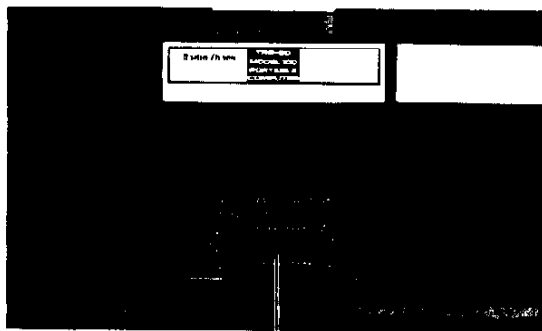
OPTIONAL RAMs   OPTIONAL ROM

Figure 7. Installing Optional RAMs and ROM

Section 8. ROM Subroutines

This section contains information on various ROM subroutines, including LCD, Keyboard, Printer, Cassette Recorder, RS-232C and Modem functions.

LCD Functions

LCD
Displays a character on the LCD at current cursor position.

> Entry Address (Hex): 4B44
> Entry conditions: A = character to be displayed
> Exit conditions: None

PLOT
Turns on pixel at specified location.

> Entry Address (Hex): 744C
> Entry conditions: D = x coordinate (0-239)
>   E = y coordinate (0-63)
> Exit conditions: None

UNPLOT
Turns off pixel at specified location.

> Entry Address (Hex): 744D
> Entry conditions: D = x coordinate (0-239)
>   E = y coordinate (0-63)
> Exit conditions: None

POSIT
Gets current cursor position.

> Entry Address (Hex): 427C
> Entry condition: None
> Exit conditions: H = column number (1-40)
>   L = row number (1-8)

ESCA
Sends specified Escape Code Sequence.

Entry Address (Hex): 4270
Entry conditions: A = escape code
Exit conditions: None

LCD Functions and Escape Codes

The routines for generating common LCD functions and escape codes have no entry or exit parameters.

Routine	Function	Entry Address (Hex)	Equiv. ESC
CRLF	Generates a Carriage Return and Line Feed	4222	—
HOME	Moves cursor to Home position (1,1)	422D	—
CLS	Clears Display	4231	—
SETSYS	Sets system line (lock line 8)	4235	T
RSTSYS	Resets system line (unlock line 8)	423A	U
LOCK	Locks display (no scrolling)	423F	Y
UNLOCK	Unlocks display (scrolling)	4244	W
CURSON	Turns on cursor	4249	P
CUROFF	Turns off cursor	424E	Q
DELLIN	Deletes line at current cursor position	4253	M
INSLIN	Inserts a blank line at cursor position	4258	L
ERAEOL	Erases from cursor to end of line	425D	K
ENTREV	Sets Reverse character mode	4269	p
EXTREV	Turns off Reverse character mode	426E	q

LCD Variable and Status Locations

Name	Contents	Entry Address
CSRY	Cursor Position (ROW)	F639
CSRX	Cursor Position (Column)	F63A
BEGLCD	Start of LCD memory	FE00
ENDLCD	End of LCD memory	FF40

Keyboard Functions

KYREAD
Scans keyboard for a key and returns with or without one.

Entry Address (Hex): 7242
Entry conditions: None
Exit conditions: A = Character, if any

      Z Flag: Set if no key found,
           reset if key found
     Carry: Set (character in code table below),
          reset (normal character set code)

When Carry is set (1), Register A will contain one of the following:

Register A	Key Pressed
0	F1
1	F2
2	F3
3	F4
4	F5
5	F6
6	F7
7	F8
8	LABEL
9	PRINT
0A	SHIFT-PRINT
0B	PASTE

CHGET
Waits and gets character from keyboard.

Entry Address (Hex): 12CB
Entry conditions: None
Exit conditions: A = character code
   Carry: Set if special character,
       reset if normal character
(F1 - F8 return preprogrammed strings)

CHSNS
Checks keyboard queue for characters.

Entry Address (Hex): 13DB
Entry conditions: None
Exit conditions: Z flag: Set if queue empty,
                 reset if keys pending

KEYX
Checks keyboard queue for characters or BREAK.

Entry Address (Hex): 7270
Entry conditions: None
Exit conditions: Z flag set if queue empty,
　　　　　　　　reset if keys pending

　　Carry: Set when BREAK entered,
　　　　　　Reset with any other key

BRKCHK
Checks for BREAK characters only (CTRL C or CTRL S).

Entry Address (Hex): 7283
Entry conditions: None
Exit conditions:
　　Carry: Set if BREAK or PAUSE entered,
　　　　　　reset if no BREAK characters

INLIN
Gets line from keyboard. Terminated by ⒺⓃⓉⒺⓇ.

Entry Address (Hex): 4644
Entry conditions: None
Exit conditions: Data stored at location F685

Using Function Key Routines

The function table consists of character strings to be used by the keyboard driver when processing Ⓕ1 - Ⓕ8 keys. The strings have a maximum length of 16 characters and are terminated by an 80 (hex) code. If the last character of the string is ORed with 80, the character will also serve as a terminator. The entire string will be placed in the keyboard buffer when the appropriate function key is pressed. You must specify character strings for all 8 function keys. (Use the terminator byte for any string you wish to ignore.)

```
Example of function table:

  FCTAB      DEFM     'Files'        ; F1
             DEFW     0D80
             DEFM     'Load'         ; F2
             DEFB     80
             DEFM     'Save'         ; F3
             DEFB     80
             DEFM     'Run'          ; F4
             DEFW     0D80
             DEFM     'List'         ; F5
             DEFW     0D80
             DEFB     80             ; Ignore F6
             DEFB     80             ; Ignore F7
             DEFM     'Menu'         ; F8
             DEFW     0D80
```

STFNK
Sets function key definitions.

Entry Address (Hex): 5A7C
Entry conditions:
    HL = Address of function table (above)
Exit conditions: None

CLRFLK
Clears function key definition table (fills table with 80s).

Entry Address (Hex): 5A79
Entry conditions: None
Exit conditions: None

DSPFNK
Displays function keys.

Entry Address (Hex): 42A8
Entry conditions: None
Exit conditions: None

STDSPF
Sets and displays function keys.

Entry Address (Hex): 42A5
Entry conditions:
    HL = Start address of function table
Exit conditions: None

ERAFNK
Erases function key display.

Entry Address (Hex): 428A
Entry conditions: None
Exit conditions: None

FNKSB
Displays function table (if enabled).

Entry Address (Hex): 5A9E
Entry conditions: None
Exit conditions: None

Printing Routines

PRINTR
Sends a character to the line printer.

Entry Address (Hex): 6D3F
Entry conditions: A = character to be printed
Exit conditions:
    Carry: Set if cancelled by BREAK,
            reset if normal return

PNOTAB
Prints character without expanding tab characters.

Entry Address (Hex): 1470
Entry conditions: A = character to be printed
Exit conditions: Unknown

PRTTAB
Prints a character expanding tabs to spaces.

Entry Address (Hex): 4B55
Entry conditions: A — character to be printed
Exit conditions: Unknown

PRTLCD
Prints contents of LCD.

Entry Address (Hex): 1E5E
Entry conditions: None
Exit conditions: None

RS232-C and Modem Routines

DISC
Disconnects phone line.

Entry Address (Hex): 52BB
Entry conditions: None
Exit conditions: None

CONN
Connects phone line.

Entry Address (Hex): 52D0
Entry conditions: None
Exit conditions: None

DIAL
Dials a specified phone number.

Entry Address (Hex): 532D
Entry conditions: HL = phone number address
Exit conditions: None

RCVX
Checks RS232 queue for characters.

Entry Address (Hex): 6D6D
Entry conditions: None
Exit conditions: A = number of characters queue
   Z flag: Set if no data, reset if characters pending

RV232C
Gets a character from RS232 receive queue.

Entry Address (Hex): 6D7E
Entry conditions: None
Exit conditions: A = character received
   Z flag: Set if O.K., reset if error (PE, FF, or OF)
   Carry: Set if BREAK pressed, else reset

SENDCQ
Sends an XON resume character (CTRL Q).

Entry Address (Hex): 6E0B
Entry conditions: None
Exit conditions: None

SENDCS
Sends an XOFF pause character (CTRL S).

Entry Address (Hex): 6E1E
Entry conditions: None
Exit conditions: None

SD232C
Sends a character to the RS-232 or Modem (with XON/XOFF).

Entry Address (Hex): 6E32
Entry conditions: A = character to be sent
Exit conditions: Unknown

CARDET
Detects carrier (for modem only).

Entry Address (Hex): 6EEF
Entry conditions: None
Exit conditions: A = 0 if carrier
    Z Flag: Set if carrier, else reset

BAUDST
Sets baud rate for RS232-C.

Entry Address (Hex): 6E75
Entry conditions: H = Baud rate (1-9,M)
Exit conditions: None

INZCOM
Initializes RS232-C and Modem.

Entry Address (Hex): 6EA6
Entry conditions:
    H = Baud rate (1-9, M)
    L = UART configuration code
        (See UART byte description below)
    Carry: Set if RS232-C, reset if modem
Exit conditions: None

Bits(s)	Description	
0	Number of Stop Bits	: 0 = 1, 1 = 2
1	Parity setting	: 0 = Odd
		1 = Even
2	Parity disable	: 0 = Enable
		1 = Disable
3-4	Word length	: 01 = 6, 10 = 7, 11 = 8

The byte is ANDed with 1FH to ignore bits 5-7. The text string containing the current STAT setting is located at F65BH (5 bytes): baud, length, parity, stop bits, and XON/XOFF switch.

SETSER
Sets serial interface parameters. Activates RS232-C/Modem.

Entry Address (Hex): 17E6
Entry conditions: HL = start address of ASCII string containing parameter terminated by zero (78E1E, 0).
    Syntax same as in Telcom's STAT
    Carry: Set for RS232-C, reset for Modem
Exit conditions: None

CLSCOM
Deactivates RS232-C/Modem.

Entry Address (Hex): 6ECB
Entry conditions: None
Exit conditions: None

Cassette Recorder Routines

DATAR
Reads character from cassette (no checksum).

Entry Address (Hex): 702A
Entry conditions: None
Exit conditions: D = character from cassette

CTON
Turns on motor.

Entry Address (Hex): 14A8
Entry conditions: None
Exit conditions: None

CTOFF
Turns off motor.

Entry Address (Hex): 14AA
Entry conditions: None
Exit conditions: None

CASIN
Reads a character from cassette and updates checksum.

Entry Address (Hex): 14B0
Entry conditions: C = current checksum
Exit conditions: A = character
                C = contains the updated checksum

CSOUT
Sends character to cassette and updates checksum.

Entry Address (Hex): 14C1
Entry conditions: A = character to be sent
                     C = current checksum
Exit conditions: C — updated checksum

SYNCW
Writes cassette header and sync byte only.

Entry Address (Hex): 6F46
Entry conditions: None
Exit conditions: None

SYNCR
Reads cassette header and sync byte only.

Entry Address (Hex): 6F85
Entry conditions: None
Exit conditions: None

DATAW
Writes a character to cassette (no checksum).

Entry Address (Hex): 6F5B
Entry conditions: A = character to be sent
Exit conditions: None

RAM File Routines

The directory table (F962) contains information on all file location, type, and status.

Each file is managed by an 11-byte directory entry in the format:

Byte 1   :   Directory Flag (for file type and status)
Bytes 2-3   :   Address of file
Bytes 4-11   :   8-byte filename

The Directory Flag contains the following information:

Bit 7 (MSB)   1 if a valid entry
Bit 6   1 for ASCII text file (DO)
Bit 5   1 for machine language (CO)
Bit 4   1 for ROM file
Bit 3   1 for invisible file
Bit 2   reserved for future use
Bit 1   reserved for future use
Bit 0   internal use only

MAKTXT
Creates a text file.

Entry Address (Hex): 220F
Entry conditions: Filename (max. 8 bytes) must be stored in FILNAM (FC93).'DO' extension not required
Exit conditions: HL = TOP address of new file
   DE = address of Directory entry (Flag)
   Carry: Set if file already exists
         Reset if new file

CHKDC
Searches for file in directory.

Entry Address (Hex): 5AA9
Entry conditions: DE = address of filename to find (ASCII filename + 0 byte terminator
Exit conditions: HL = start address (TOP) of file
   Z Flag: 0 (file found)
         1 (file not found)

GTXTTB
Gets top address of file.

Entry Address (Hex): 5AE3
Entry conditions: HL = address of directory entry for file
Exit conditions: HL = TOP start address of file

KILASC
Kills a text (DO) file.

Entry Address (Hex): 1FBE
Entry conditions: DE = file TOP start address
           HL = address of directory entry (flag)
Exit conditions: None

INSCHR
Inserts a character in a file.

Entry Address (Hex): 6B61
Entry conditions: A = character to insert
           HL = address to insert character
Exit conditions: HL = HL + 1
   Carry: Set if out of memory

MAKHOL
Inserts a specified number of spaces in a file.

Entry Address (Hex): 6B6D
Entry conditions: BC = number of spaces to insert
                 HL = address to insert spaces
Exit conditions: HL and BC are preserved
   Carry: Set if out of memory

MASDEL
Deletes specified number of characters.

Entry Address (Hex): 6B9F
Entry conditions: BC = number of characters to delete
                 HL = address of deletion
Exit conditions: HL and BC are preserved

Other Routines

INITIO
Cold start reset.

Entry Address (Hex): 6CD6
Entry conditions: None
Exit conditions: None

IOINIT
Warm start reset.

Entry Address (Hex): 6CE0
Entry conditions: None
Exit conditions: None

MENU
Goes to Main Menu.

Entry Address (Hex): 5797
Entry conditions: None
Exit conditions: None

MUSIC
Makes tone.

Entry Address (Hex): 72C5
Entry conditions: DE = frequency (See Owner's manual)
                 B = duration (See Owner's manual)
Exit conditions: None

TIME
Reads system TIME.

Entry Address (Hex): 190F
Entry conditions: HL = address of 8-byte area for TIME
Exit conditions: HL ⇒ TIME (hh:mm:ss)

DATE
Reads system DATE.

Entry Address (Hex): 192F
Entry conditions: HL = address of 8-byte area for DATE
Exit conditions: HL ⇒ DATE (mm/dd/yy)

DAY
Reads system DAY of the week.

Entry Address (Hex): 1962
Entry conditions: HL = address of 3 byte area for DAY
Exit conditions: HL ⇒ DAY (ddd)

Section 9. Character Code Table

ASCII Character Code Tables

Decimal	Hex	Binary	Printed Character	Keyboard Character
0	00	00000000		CTRL @
1	01	00000001		CTRL A
2	02	00000010		CTRL B
3	03	00000011		CTRL C
4	04	00000100		CTRL D
5	05	00000101		CTRL E
6	06	00000110		CTRL F
7	07	00000111		CTRL G
8	08	00001000		CTRL H
9	09	00001001		CTRL I
10	0A	00001010		CTRL J
11	0B	00001011		CTRL K
12	0C	00001100		CTRL L
13	0D	00001101		CTRL M
14	0E	00001110		CTRL N
15	0F	00001111		CTRL O
16	10	00010000		CTRL P
17	11	00010001		CTRL Q
18	12	00010010		CTRL R
19	13	00010011		CTRL S
20	14	00010100		CTRL T
21	15	00010101		CTRL U
22	16	00010110		CTRL V
23	17	00010111		CTRL W
24	18	00011000		CTRL X
25	19	00011001		CTRL Y
26	1A	00011010		CTRL Z
27	1B	00011011		ESC
28	1C	00011100		⊟
29	1D	00011101		⊟
30	1E	00011110		⊞
31	1F	00011111		⊞
32	20	00100000		SPACEBAR
33	21	00100001	!	!
34	22	00100010	"	"
35	23	00100011	#	#

Decimal	Hex	Binary	Printed Character	Keyboard Character
36	24	00100100	$	$
37	25	00100101	%	%
38	26	00100110	&	&
39	27	00100111	'	'
40	28	00101000	(	(
41	29	00101001	)	)
42	2A	00101010	*	*
43	2B	00101011	+	+
44	2C	00101100	,	,
45	2D	00101101	–	–
46	2E	00101110	.	.
47	2F	00101111	/	/
48	30	00110000	0	0
49	31	00110001	1	1
50	32	00110010	2	2
51	33	00110011	3	3
52	34	00110100	4	4
53	35	00110101	5	5
54	36	00110110	6	6
55	37	00110111	7	7
56	38	00111000	8	8
57	39	00111001	9	9
58	3A	00111010	:	:
59	3B	00111011	;	;
60	3C	00111100	<	<
61	3D	00111101	=	=
62	3E	00111110	>	>
63	3F	00111111	?	?
64	40	01000000	@	@
65	41	01000001	A	A
66	42	01000010	B	B
67	43	01000011	C	C
68	44	01000100	D	D
69	45	01000101	E	E
70	46	01000110	F	F

* For uppercase letters A-Z, press SHIFT or CAPS LOCK before pressing the Keyboard Character.

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Decimal	Hex	Binary	Printed Character	Keyboard Character
71	47	01000111	G	G
72	48	01001000	H	H
73	49	01001001	I	I
74	4A	01001010	J	J
75	4B	01001011	K	K
76	4C	01001100	L	L
77	4D	01001101	M	M
78	4E	01001110	N	N
79	4F	01001111	O	O
80	50	01010000	P	P
81	51	01010001	Q	Q
82	52	01010010	R	R
83	53	01010011	S	S
84	54	01010100	T	T
85	55	01010101	U	U
86	56	01010110	V	V
87	57	01010111	W	W
88	58	01011000	X	X
89	59	01011001	Y	Y
90	5A	01011010	Z	Z
91	5B	01011011	[	[
92	5C	01011100	\	(GRPH) −
93	5D	01011101	]	]
94	5E	01011110	^	^
95	5F	01011111	_	_
96	60	01100000	\	(GRAPH) [
97	61	01100001	a	A
98	62	01100010	b	B
99	63	01100011	c	C
100	64	01100100	d	D
101	65	01100101	e	E
102	66	01100110	f	F
103	67	01100111	g	G
104	68	01101000	h	H
105	69	01101001	i	I
106	6A	01101010	j	J
107	6B	01101011	k	K
108	6C	01101100	l	L
109	6D	01101101	m	M
110	6E	01101110	n	N
111	6F	01101111	o	O
112	70	01110000	p	P
113	71	01110001	q	Q
114	72	01110010	r	R
115	73	01110011	s	S
116	74	01110100	t	T
117	75	01110101	u	U
118	76	01110110	v	V
119	77	01110111	w	W
120	78	01111000	x	X
121	79	01111001	y	Y
122	7A	01111010	z	Z
123	7B	01111011	{	(GRPH) 9
124	7C	01111100	|	(GRPH) _
125	7D	01111101	}	(GRPH) 0
126	7E	01111110	~	(GRPH)]
127	7F	01111111		(DEL)
128	80	10000000	☎	(GRPH) p
129	81	10000001		(GRPH) m
130	82	10000010		(GRPH) f
131	83	10000011		(GRPH) x
132	84	10000100		(GRPH) c
133	85	10000101	✝	(GRPH) a
134	86	10000110		(GRPH) h
135	87	10000111		(GRPH) t
136	88	10001000	i	(GRPH) l
137	89	10001001	√	(GRPH) r
138	8A	10001010	≠	(GRPH) /
139	8B	10001011	Σ	(GRPH) s
140	8C	10001100	≈	(GRPH) '
141	8D	10001101	±	(GRPH) =
142	BE	10001110	∫	(GRPH) i
143	BF	10001111	◄	(GRPH) e
144	90	10010000		(GRPH) y
145	91	10010001		(GRPH) u
146	92	10010010		(GRPH) ;
147	93	10010011		(GRPH) q
148	94	10010100		(GRPH) w
149	95	10010101	♂	(GRPH) b
150	96	10010110	♀	(GRPH) n
151	97	10010111	‰	(GRPH)
152	98	10011000	↑	(GRPH) o
153	99	10011001	↓	(GRPH) ,
154	9A	10011010	→	(GRPH) l
155	9B	10011011	←	(GRPH) k
156	9C	10011100	∞	(GRPH) 2
157	9D	10011101	◊	(GRPH) 3
158	9E	10011110	♡	(GRPH) 4
159	9F	10011111	♤	(GRPH) 5
160	A0	10100000		(CODE) '
161	A1	10100001	à	(CODE) x
162	A2	10100010	ç	(CODE) c
163	A3	10100011	£	(GRPH) 8
164	A4	10100100		(CODE) "
165	A5	10100101	µ	(CODE) M
166	A6	10100110	°	(CODE))
167	A7	10100111	▼	(CODE) _
168	A8	10101000	†	(CODE) +
169	A9	10101001		(CODE) s
170	AA	10101010		(CODE) R
171	AB	10101011		(CODE) C
172	AC	10101100	¼	(CODE) p
173	AD	10101101	¾	(CODE) ;
174	AE	10101110	½	(CODE) /
175	AF	10101111	¶	(CODE) 0

* For lowercase letters a-z, be sure (CAPS LOCK) is not pressed "down."

Decimal	Hex	Binary	Printed Character	Keyboard Character
176	B0	10110000	¥	(GRPH) 7
177	B1	10110001	Â	(CODE) A
178	B2	10110010	Ô	(CODE) O
179	B3	10110011	Û	(CODE) U
180	B4	10110100	¢	(GRPH) 6
181	B5	10110101	ˉ	(CODE) [
182	B6	10110110	ä	(CODE) a
183	B7	10110111	ö	(CODE) o
184	B8	10111000	ü	(CODE) u
185	B9	10111001	ß	(CODE) S
186	BA	10111010	™	(CODE) T
187	BB	10111011	é	(CODE) d
188	BC	10111100	ù	(CODE) ,
189	BD	10111101	è	(CODE) v
190	BE	10111110	¨	(CODE) =
191	BF	10111111	£	(CODE) F
192	C0	11000000	à	(CODE) I
193	C1	11000001	ê	(CODE) 3
194	C2	11000010	î	(CODE) 8
195	C3	11000011	ô	(CODE) 9
196	C4	11000100	û	(CODE) 7
197	C5	11000101	˙	(CODE) −
198	C6	11000110	ë	(CODE) e
199	C7	11000111	ï	(CODE) i
200	C8	11001000	á	(CODE) q
201	C9	11001001	í	(CODE) k
202	CA	11001010	ó	(CODE) l
203	CB	11001011	ú	(CODE) j
204	CC	11001100	ý	(CODE) y
205	CD	11001101	ñ	(CODE) n
206	CE	11001110	ã	(CODE) z
207	CF	11001111	õ	(CODE) .
208	D0	11010000	Á	(CODE) !
209	D1	11010001	É	(CODE) #
210	D2	11010010	Í	(CODE) *
211	D3	11010011	Ó	(CODE) (
212	D4	11010100	Ú	(CODE) &
213	D5	11010101	ï	(CODE) l
214	D6	11010110	Ë	(CODE) E
215	D7	11010111	É	(CODE) D

Decimal	Hex	Binary	Printed Character	Keyboard Character
216	D8	11011000	Á	(CODE) Q
217	D9	11011001	ì	(CODE) K
218	DA	11011010	Ó	(CODE) L
219	DB	11011011	Ú	(CODE) J
220	DC	11011100	Ý	(CODE) Y
221	DD	11011101	Ù	(CODE) <
222	DE	11011110	Ė	(CODE) V
223	DF	11011111	À	(CODE) X
224	ED	11100000		(GRPH) Z
225	E1	11100001	▪ (upper left)	(GRPH) !
226	E2	11100010	▪ (upper right)	(GRPH) α
227	E3	11100011	▪ (lower left)	(GRPH) #
228	E4	11100100	▪ (lower right)	(GRPH) $
229	E5	11100101	▜	(GRPH) %
230	E6	11100110	▟	(GRPH) ^
231	E7	11100111	▬ (upper)	(GRPH) Q
232	E8	11101000	▬ (lower)	(GRPH) W
233	E9	11101001	▮ (left)	(GRPH) E
234	EA	11101010	▮ (right)	(GRPH) R
235	EB	11101011	▛	(GRPH) A
236	EC	11101100	▜	(GRPH) S
237	ED	11101101	▙	(GRPH) D
238	EE	11101110	▟	(GRPH) F
239	EF	11101111	■	(GRPH) X
240	F0	11110000	⌐	(GRPH) U
241	F1	11110001	─	(GRPH) P
242	F2	11110010	¬	(GRPH) O
243	F3	11110011	⊤	(GRPH) I
244	F4	11110100	⊢	(GRPH) J
245	F5	11110101	│	(GRPH) :
246	F6	11110110	└	(GRPH) M
247	F7	11110111	┘	(GRPH) >
248	F8	11111000	⊥	(GRPH) <
249	F9	11111001	┤	(GRPH) L
250	FA	11111010	+	(GRPH) K
251	FB	11111011	◢	(GRPH) H
252	FC	11111100	◣	(GRPH) T
253	FD	11111101	◥	(GRPH) G
254	FE	11111110	◤	(GRPH) Y
255	FF	11111111	▓	(GRPH) C

Section 10. Description of LSIs

This section contains a description of the following LSI ICs:

- **MSM80C85ARS (CPU)**
- **MSM81C55RS (PIO)**
- **IM6402 (UART)**
- **µPD1990AC (TIMER)**

- **MC14412 (MODEM)**
- **TC5518BF-25 (RAM)**
- **LH-535618 (ROM)**

MSM80C85ARS (CPU)

MSM80C85ARS (80C85) is a one-chip, 8-bit parallel Central Processing Unit (CPU). Its instruction set is fully compatible with the 8080A microprocessor.
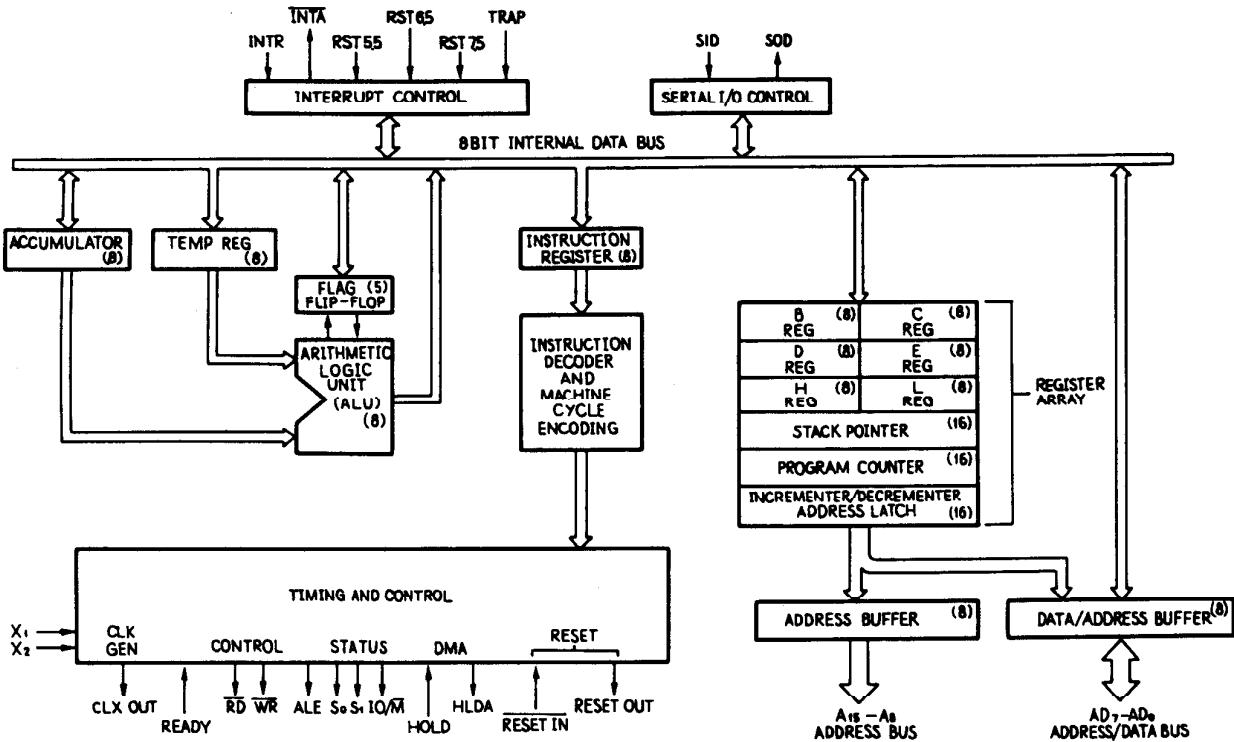
Figure 10-1. 80C85 CPU Functional Block Diagram

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The figure below shows the pin layout of the microprocessor:


```
            X₁ [1]              [40] Vcc
            X₂ [2]              [39] HOLD
     RESET OUT [3]              [38] HLDA
           SOD [4]              [37] CLK (OUT)
           SID [5]              [36] RESET IN
          TRAP [6]              [35] READY
         RST7.5 [7]             [34] IO/M̄
         RST6.5 [8]             [33] S₁
         RST5.5 [9]             [32] R̄D̄
          INTR [10]   MSM80C85A [31] W̄R̄
          ĪNTA [11]             [30] ALE
          AD₀ [12]              [29] S₀
          AD₁ [13]              [28] A₁₅
          AD₂ [14]              [27] A₁₄
          AD₃ [15]              [26] A₁₃
          AD₄ [16]              [25] A₁₂
          AD₅ [17]              [24] A₁₁
          AD₆ [18]              [23] A₁₀
          AD₇ [19]              [22] A₉
          GND [20]              [21] A₈
```
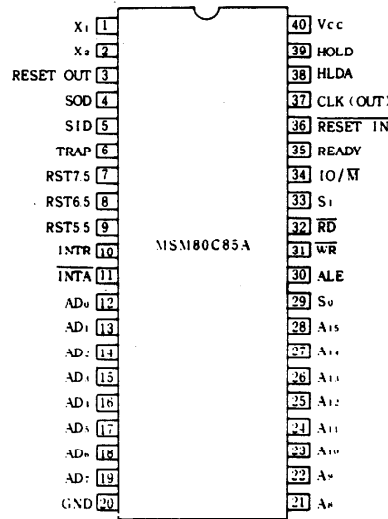
Figure 10-2. 80C85 Pinout Diagram

80C85 Functional Pin Description

Symbol	Function

A_8 - A_{15}
(Output, 3-state)

Address Bus: Most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

AD_{0-7}
(Input/Output, 3-state)

Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

ALE
(Output)

Address Latch Enable: Occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.

S_0, S_1, and
IO/M̄ (Output)

Machine cycle status:

IO/M̄	S_1	S_0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

* = 3-state (high impedance)
X = unspecified

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Symbol	Function
	S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0, and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. Three-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer (internal processing can continue). The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the CPU has received the HOLD request and will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one-half clock after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST is used as a general purpose interrupt and sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle, a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$ (Output)	INTERRUPT ACKNOWLEDGE is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART interrupts have same timing as INTR, but cause the automatic insertion of an internal RESTART. The priority of these interrupts, which have a higher priority than INTR, is ordered as shown in Table 10-1. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	TRAP interrupt is a nonmaskable RESTART interrupt, also recognized as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable and has the highest priority of any interrupt. (See Table 10-1.)

Symbol	Function
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an RC network for power-on RESET delay. The CPU is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates the CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line: Data on this line is loaded into accumulator bit 7 when a RIM instruction is executed.
SOD (Output)	Serial output data line: Output SOD is set or reset as specified by the SIM instruction.
Vcc	+5 volt supply.
GND	Ground reference.

Name	Priority	Address Branched to (1) when Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2)	High level until sampled.

Table 10-1. 80C85 Interrupt Priority, RESTART, ADDRESS, and Sensitivity

Notes:

1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.

Functional Description

80C85 has twelve addressable 8-bit registers. Four function only as two 16-bit register pairs. Six can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 80C85 register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers: data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

80C85 uses a multiplexed data bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

80C85 provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and $IO/\overline{M}$ signals for bus control. An Interrupt Acknowledge signal $(\overline{INTA})$ is also provided. HOLD, READY, and all interrupts are synchronized with the processor's internal clock. 80C85 also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, 80C85 has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

Interrupt and Serial I/O

80C85 has five interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt, but nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks (See Table 10-1).

There are two types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are **high level-sensitive** like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is **rising edge-sensitive**.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then, it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 80C85. RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

Status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$.

Interrupts are arranged in a fixed priority that determines which interrupt is to be recognized (if more than one is pending) as follows: TRAP — highest priority; RST 7.5, RST 6.5, RST 5.5, INTR — lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. TRAP input is recognized just as any other interrupt, but has the highest priority. It is not affected by any flag or mask and is both edge and level sensitive. TRAP input must go high and remain high until acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 10-3 illustrates the TRAP interrupt request circuitry within the 80C85. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.
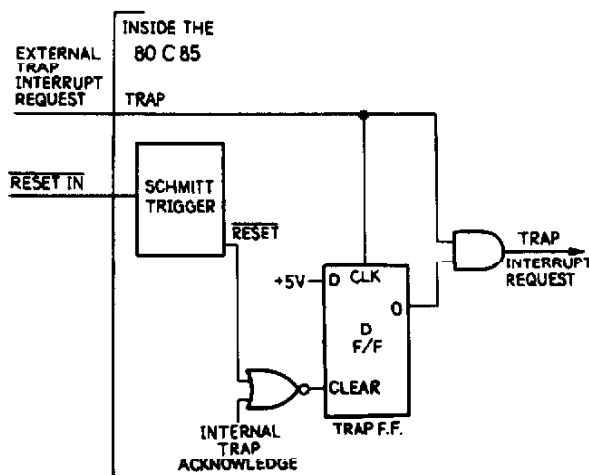
Figure 10-3. TRAP and RESET In Circuit

Although TRAP disables interrupts, it preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5-7.5 will provide current Interrupt Enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is ready by RIM, and SIM sets the SOD data.

Basic System Timing

80C85 has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8 bits of address on the Data Bus. Figure 10-4 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O, port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these takes place is defined by the status of the three status lines (IO/$\overline{\text{M}}$, S_1, S_0) and the three control signals $\overline{\text{RD}}$, $\overline{\text{WR}}$, and $\overline{\text{INTA}}$ (see Table 10-2). The status lines can be used as advanced controls (for example, device selection), since they become active at the T_1 state at the outset of each machine cycle. Control lines $\overline{\text{RD}}$ and $\overline{\text{WR}}$ become active later, at the time the transfer of data is to take place, and are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the reception of READY or HOLD inputs). Any T state must be one of ten possible states, shown in Table 10-3.

MACHINE CYCLE		STATUS			CONTROL		
		$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)	0	1	1	0	1	1
MEMORY READ	(MR)	0	1	0	0	1	1
MEMORY WRITE	(MW)	0	0	1	1	0	1
I/O READ	(IOR)	1	1	0	0	1	1
I/O WRITE	(IOW)	1	0	1	1	0	1
ACKNOWLEDGE of INTR	(INA)	1	1	1	1	1	0
BUS IDLE (BI):	DAD	0	1	0	1	1	1
	ACK, of RST, TRAP	1	1	1	1	1	1
	HALT	TS	0	0	TS	TS	1

Table 10-2. 80C85 Machine Cycle Chart

Machine Strate	Status & Buses				Control		
	S_1, S_0	$IO/\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}, \overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"   1 = Logic "1"   TS = High Impedance   X = Unspecified
* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
† $IO/M = 1$ during $T_4 - T_6$ of INA machine cycle.

Table 10-3. 80C85 Machine State Chart
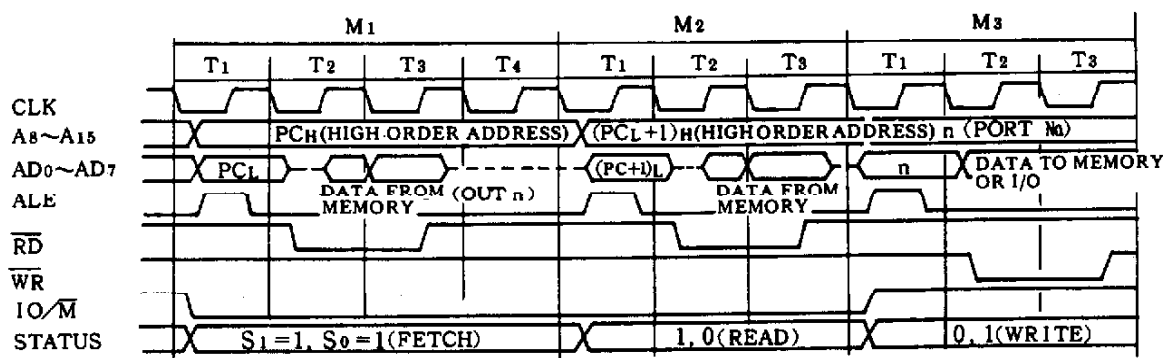
Figure 10-4. 80C85 Basic System Timing

Ambient Temperature Under Bias	−40°C to +85°C
Storage Temperature	−55°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5°C to +7V
Power Dissipation	1.0 Watt

Table 10-4. Absolute Maximum Ratings

80C85 Waveform
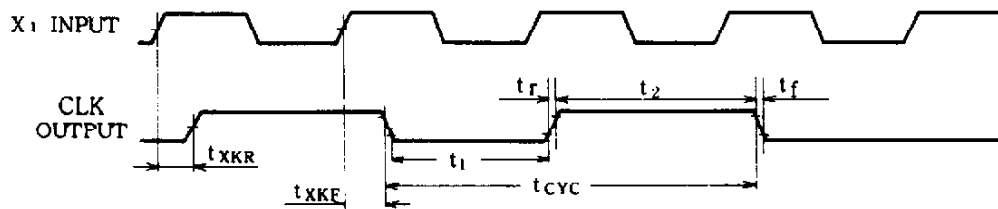
Figure 10-5. 80C85 Clock Timing Waveform

Read Operation
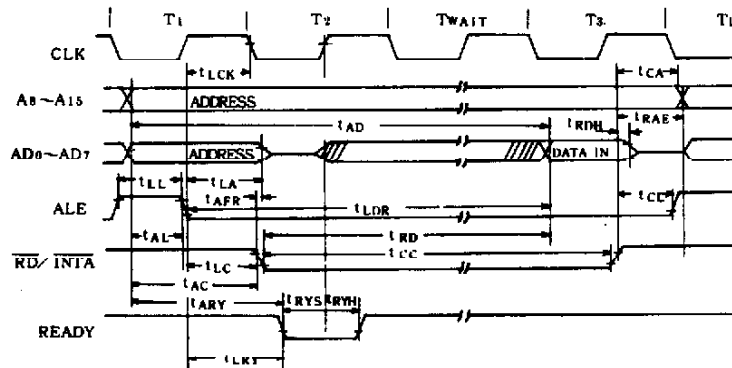
Write Operation
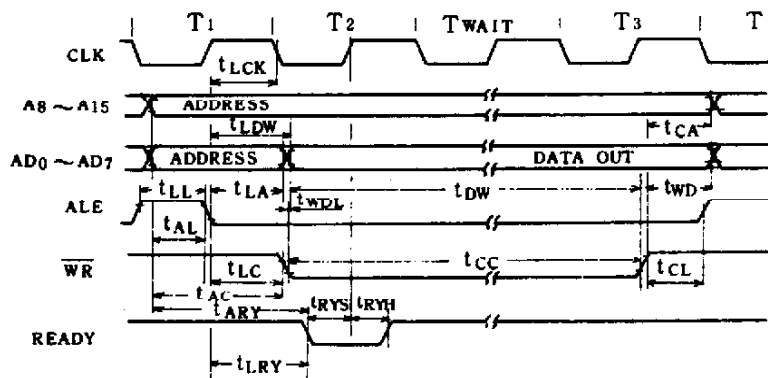
Read Operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation

Figure 10-6. 80C85 Bus Timing
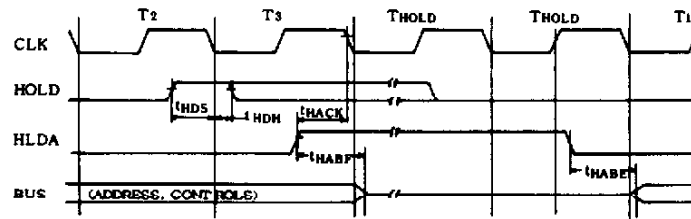
Figure 10-7. Hold Timing
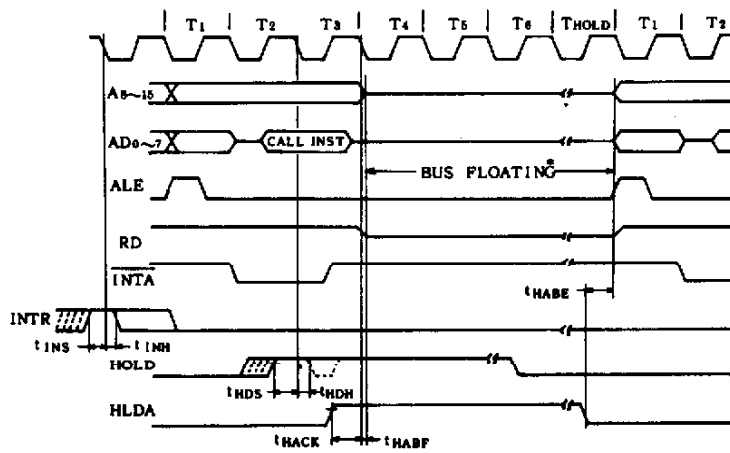
* IO/M is also floating during this time.

Figure 10-8. 80C85 Interrupt and Hold Timing

MSM81C55RS (PIO)

C-MOS, 2048-bit STATIC RAM with I/O ports and Timer. The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed as status pins, thus allowing the remaining two ports to operate in the handshake mode.

A 14-bit programmable counter/timer is also included on the chip to provide either a square wave or terminal count pulse for the CPU system, depending on the timer mode.

81C55 RAM is not used in Model 100. A timer/counter is used as the clock generator necessary for communication and to generate the melody.

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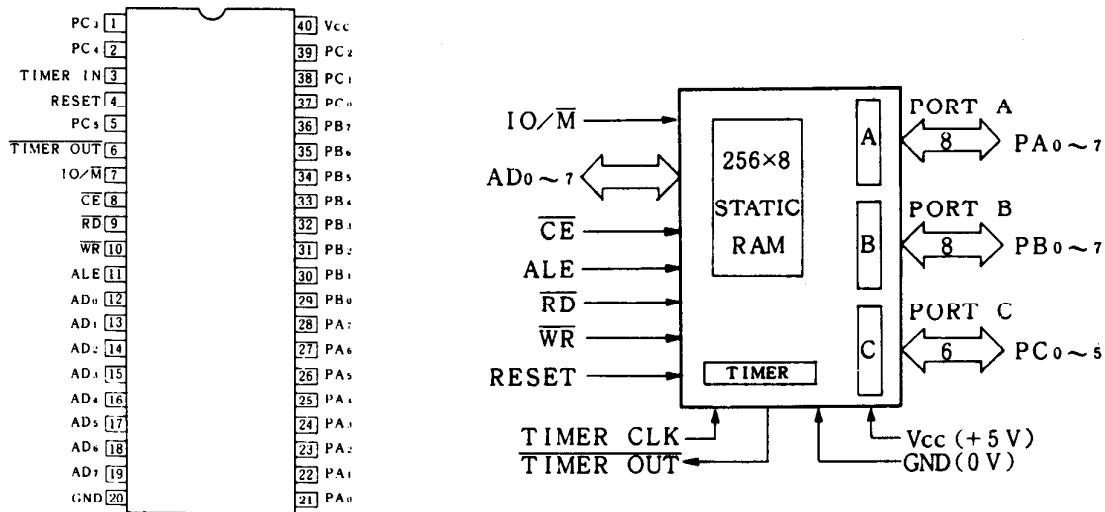
Figure 10-9. Pin Configuration and Block Diagram

81C55 Pin Functions

Symbol	Function
RESET (Input)	Pulse provided by the 80C85 to initialize the system (connect to 80C85 RESET OUT). A high input on this line resets the chip and initializes the three I/O ports to input mode. Width of the RESET pulse should typically be two 80C85 clock cycle times.
AD_{0-7} (Input)	Three-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside 81C55 on the falling edge of ALE. The address can be either for the memory section or the I/O section, depending on the $IO/\overline{M}$ input. 8-bit data is either written into the chip or read from the chip, depending on $\overline{WR}$ or $\overline{RD}$ input signal.
CE (Input)	Chip Enable: $\overline{CE}$ is ACTIVE LOW.
$\overline{RD}$ (Input)	Read control: Input low on this line with the Chip Enable active enables AD_{0-7} buffers. If the $IO/\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (Input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on the $IO/\overline{M}$.
ALE	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and $IO/\overline{M}$ into the chip at the falling edge of ALE.
$IO/\overline{M}$ (Input)	Selects the memory if low, and the command/status registers if high.

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Symbol	Function
PA$_{0-7}$ (8) (Input/Output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB$_{0-7}$ (8) (Input/Output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC$_{0-5}$ (6) (Input/Output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When used as control signals, PC$_{0-5}$ provide the following: PC$_0$ — A INTR (Port A Interrupt) PC$_1$ — $\overline{ABF}$ (Port A Buffer Full) PC$_2$ — $\overline{A\ STB}$ (Port A Strobe) PC$_3$ — B INTR (Port B Interrupt) PC$_4$ — $\overline{B\ BF}$ (Port B Buffer Full) PC$_5$ — B STB (Port B Strobe)
TIMER IN (Input)	Input to the counter-timer.
$\overline{\text{TIMER OUT}}$ (Output)	Timer output. This output can be either a square wave or a pulse, depending on the timer mode.
Vcc	+5 volt supply.
GND	Ground reference.

81C55 Waveform

Read Cycle
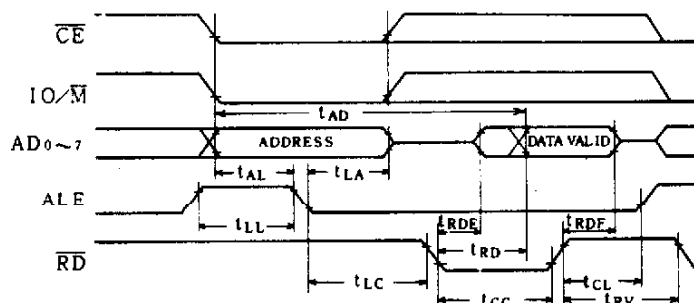
Write Cycle
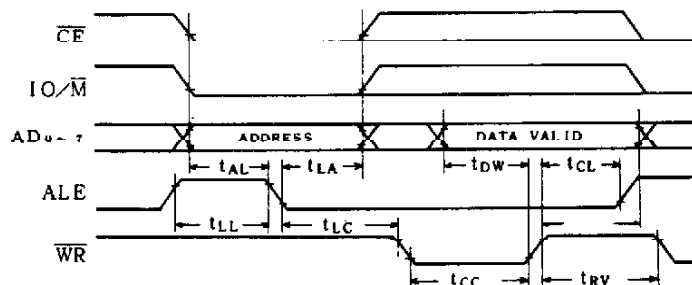
Figure 10-10. 81C55 Read/Write Timing Diagram

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81C55 Strobed I/O Timing

Strobed Input Mode
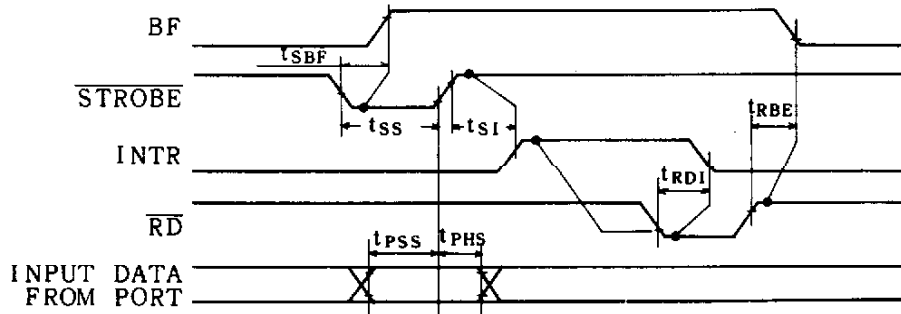
Strobed Output Mode
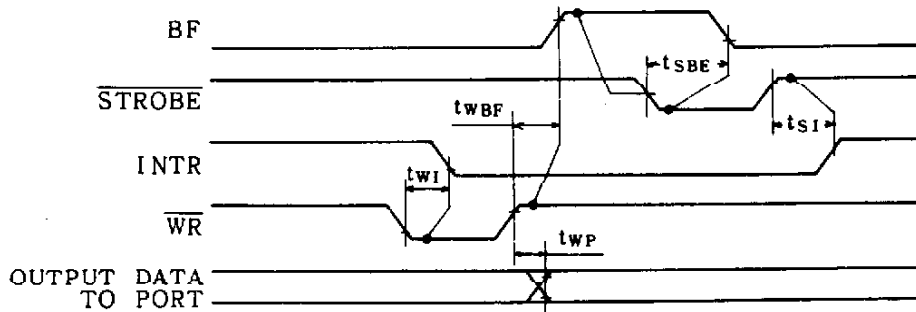
Figure 10-11. 81C55 Strobed I/O Timing

81C55 Basic I/O Timing

Basic Input Mode
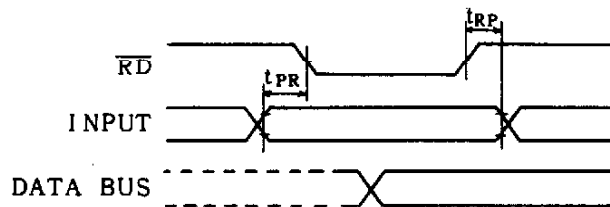
Basic Output Mode
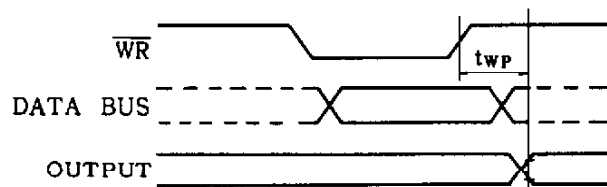
Figure 10-12. Basic I/O Timing
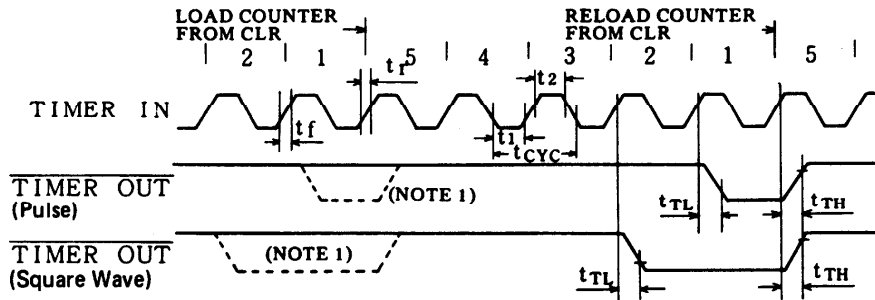
NOTE 1. The timer output is periodic if in an automatic reload mode (M1 MODE BIT = 1)

Figure 10-13. Timer Output Waveform Countdown from 5 to 1

IM6402 (UART)

IM6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity, and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

Data word length can be 5, 6, 7, or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. Stop bits may be one or two or one and one-half when transmitting a 5-bit code.

IM6402 can be used in a wide range of applications, including modems, printers, peripherals, and remote data acquisition systems. CMOS/LSI technology permits operation clock frequencies up to 2.0 MHz (125K baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300 mW to 10 mW. Status logic increases flexibility and simplifies the user interface.
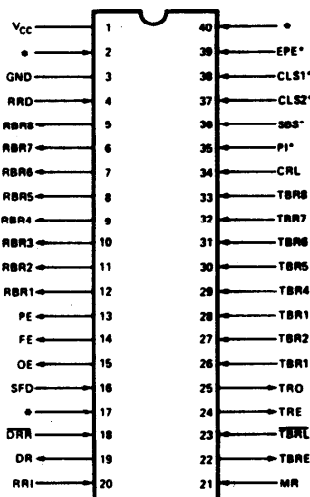
* Shown in Table C-5

Figure 10-14. IM6402 Pin Layout

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CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

Table 10-5. IM6402 Control Word Format
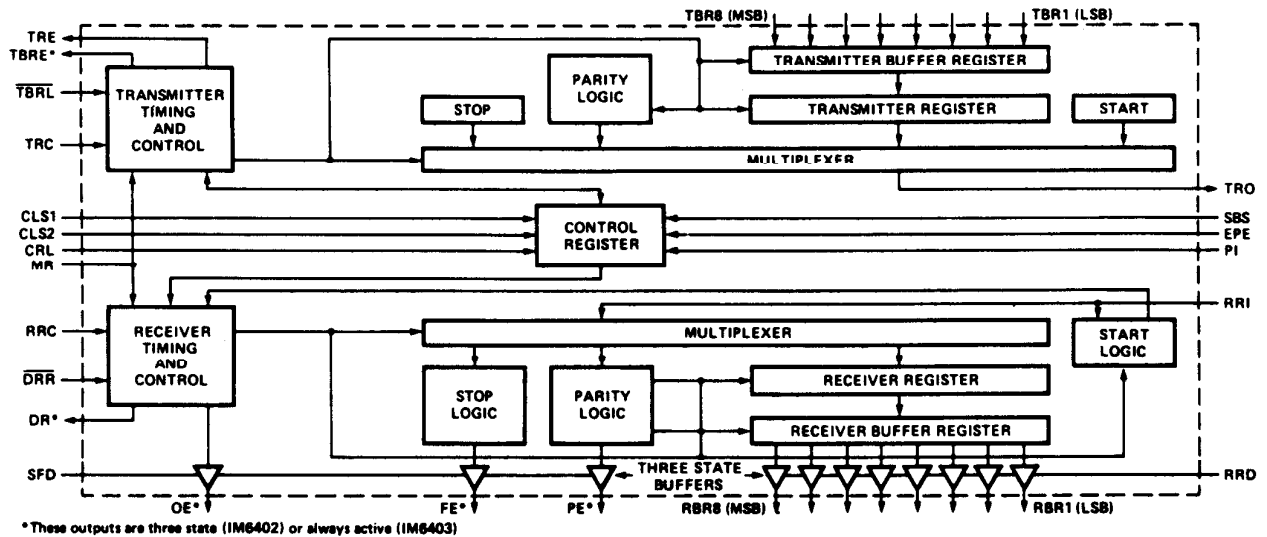
Figure 10-15. IM6402 Functional Block Diagram

* These outputs are three state (IM6402) or always active (IM6403)

IM6402 Pin Functions

Symbol	Description
Vcc	Positive voltage supply
NC	No connection
GND	Ground
RRD	High level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1-RBR8 to a high impedance state.

Symbol	Description
RBR8	Contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats of less than 8 characters are justified to RBR1.
RBR7	See Pin 5 - RBR8
RBR6	See Pin 5 - RBR8
RBR5	See Pin 5 - RBR8
RBR4	See Pin 5 - RBR8
RBR3	See Pin 5 - RBR8
RBR2	See Pin 5 - RBR8
RBR1	See Pin 5 - RBR8
PE	High level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited, this output is low.
FE	High level on FRAMING ERROR indicates the first stop bit was invalid.
OE	High level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the received buffer register.
SFD	High level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
RRC	RECEIVER REGISTER CLOCK is 16X the receiver data rate.
DRR	Low level on DATA RECEIVED RESET clears the data received output DR to a low level.
DR	High level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
MR	High level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles. MR does not clear the receiver buffer register. This input must be pulsed at least once after power-up.
TBRE	High level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
TBRL	Low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register is busy Transfer is automatically delayed so that the two characters are transmitted end to end.

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Symbol	Description
TRE	High level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character, including stop bits.
TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
TBR2	See Pin 26 - TBR1
TBR3	See Pin 26 - TBR1
TBR4	See Pin 26 - TBR1
TBR5	See Pin 26 - TBR1
TBR6	See Pin 26 - TBR1
TBR7	See Pin 26 - TBR1
TBR8	See Pin 26 - TBR1
CRL	High level on CONTROL REGISTER LOAD loads the control register.
PI	High level on PARITY INHIBIT inhibits parity generation. Parity checking and forces PE output low.
SBS	High level on STOP BIT SELECT selects 1.5 stop bits for 5-character format and 2 stop bits for other lengths.
CLS2	These inputs program the CHARACTER LENGTH SELECTED — CLS1 low CLS2 low, 5 bits; CLS1 high CLS2 low, 6 bits; CLS1 low CLS2 high, 7 bits; CLS1 high CLS2 high, 8 bits.
CLS1	See Pin 37 - CLS2.
EPE	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
TRC	TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

μPD1990AC (TIMER)

μPD1990AC is a CMOS integrated circuit with a clock function designed for connection to a microcomputer.

This IC independently measures the month, date, day of the week, hour, minute, and second, and inputs and outputs time data freely upon command from the microprocessor. By employing this IC, the microprocessor is freed from performing clock functions and can be devoted exclusively to other complex operations.

μPD1990C employs the oscillation of a 32.768 kHz crystal as a reference. All functions are enclosed in a 14-pin dual in-line package.

Features

● Measures time (hours, minutes, and seconds) and calendar (months, data, and day of the week).

● Inputs and outputs serial data. (Input and output code: all digits are binary coded decimals, except the month, which is a hexadecimal code.)

● Generates reference frequency of 32.768 kHz through the crystal oscillator circuit.

● Provides timing pulse outputs. (Selection of 64 Hz, 256 Hz, or 2048 Hz is possible.)

● Makes multi-chip applications possible by using the CS (chip selection) terminal.

Specifications

Reference frequency (XTAL osc.)	32.768 kHz
Date	Hours, minutes, seconds, months, data, and days of the week ("hours" by 24-hour system) with automatic adjustment of long and short months)
Data (serial input/output and clock)	Data input and output in synchronization with the clock input from CLK.
Time pulse output	Either 64, 256, or 2048 Hz can be selected by command.
Mode selection	Selected according to input C_0-C_2. $C_2 = 0$ Register control (control of data input/output). $C_2 = 1$ TP control (control of time pulses) and test control (control of test mode). Commands are latched by the STB (strobe) input.
Chip select	CLK and STB inputs are prohibited by CS input.
Prohibition of data output	DATA OUT terminal will become high impedance when the OUT ENABL is input. Has no relation with other actions).

Terminals

Input terminals

DATA IN	Data input of 40-bit shift register
CLK	Shift clock input of 40-bit shift register
C_0-C_2	Command input (3-bit)
STB	Strobe input
CS	Chip select input (prohibits CLS and STB)
OUT ENBL	Output control input (makes the DATA OUT high impedance by inputting low level).

Output terminals

DATA OUT	Data output of 40-bit shift register.
TP	Time pulse output.

Oscillation terminals

XTAL 1	Oscillation inverter input (OSC IN).
XTAL 2	Oscillation inverter output (OSC OUT).

Power supply terminals

VDD   Plus power supply

GND (Vss)   Common line
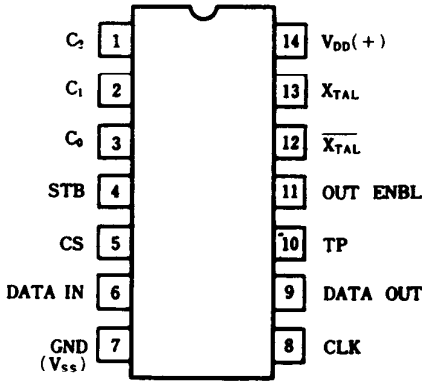
Figure 10-16. μPD1990AC Pin Layout

Block Diagram

SD : Serial Data
PS : Preset
D/W: Day of the Week
CS : Chip Select
TP : Timing Pulse
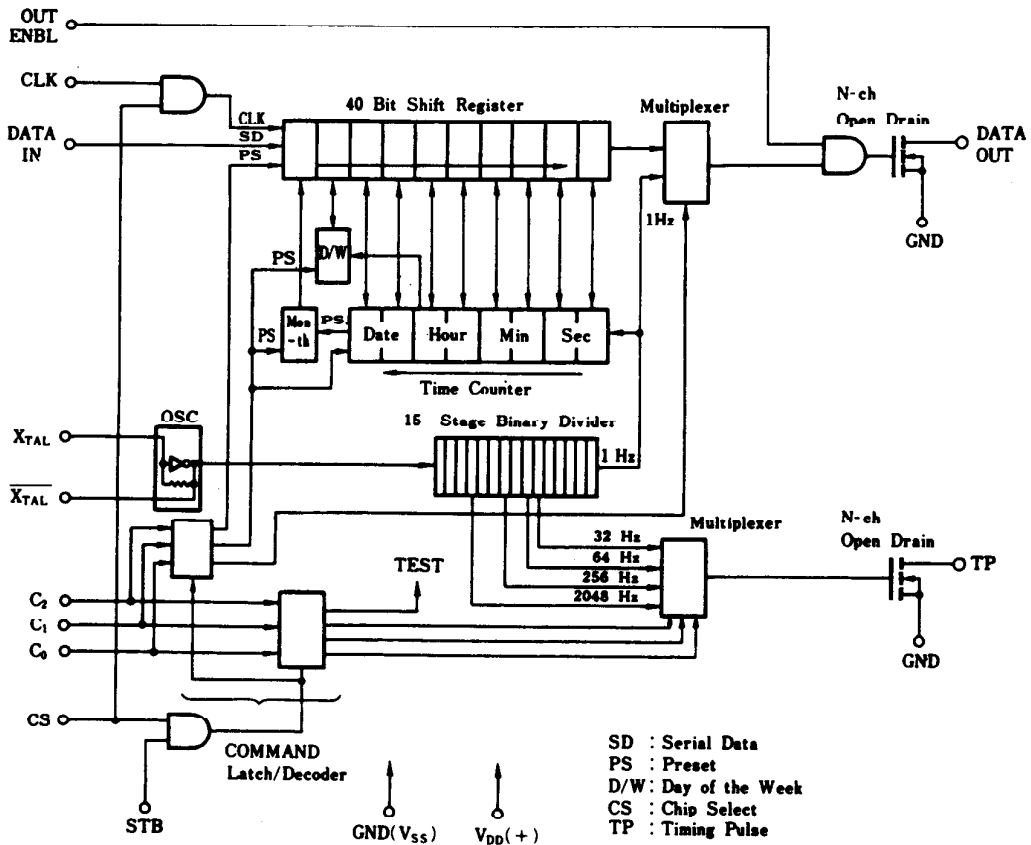
Figure 10-17. μPD1990AC Block Diagram

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Command Input Timing Diagram

t_{dC-O} : 2 μs MAX. (R_L=33 kΩ. C_L=15 pF)
t_{DSU} : 2 μs MIN.
t_{DHLD} : 2 μs MIN.
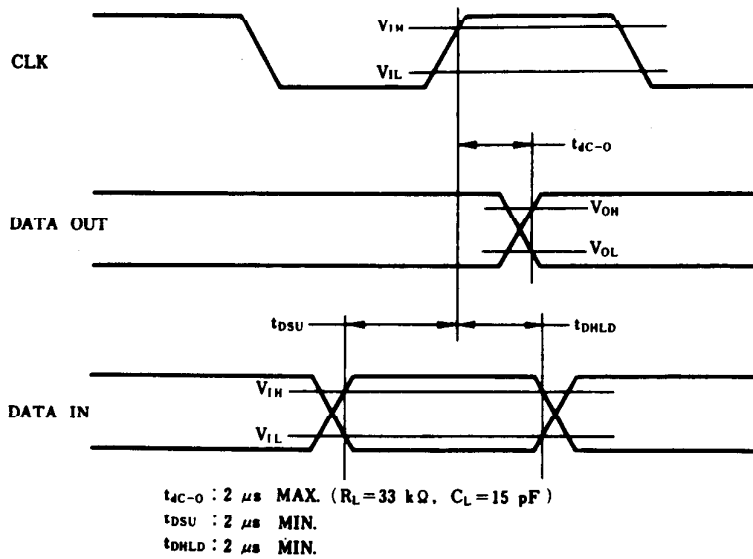
Figure 10-18. μPD1990AC Command Input Timing Diagram

Commands designated by C_0. C_1. and C_2 will be written into the latch when the STB terminal becomes high level, and will be held until a different command of the same group is written in.

Data Input/Output Timing Diagram

Written-in data LSB ("H")
appears at output
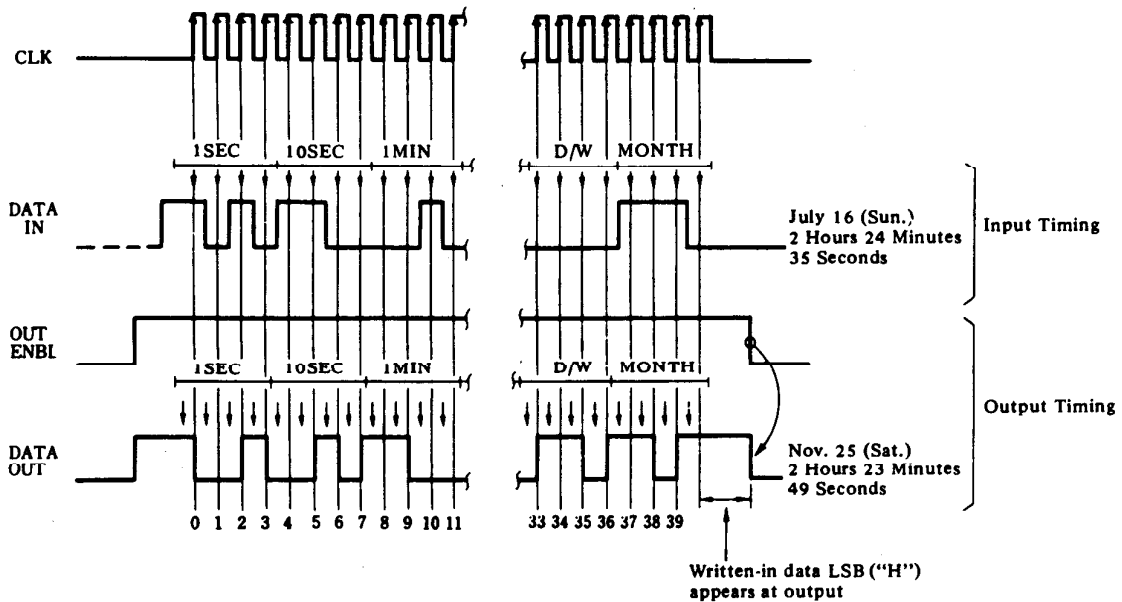
Figure 10-19. μPD1990AC Data Input/Output Timing Diagram

MC14412 (MODEM)

Figure 10-22 shows the MODEM in a system application. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified before dividing the 600 ohm telephone line.

The FSK signal from the remote MODEM is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal.

The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

Pin Functions

Symbol	Function
TYPE	TYPE input selects either the U.S. or C.I.T.T. operational frequencies for both transmitting and receiving data. When TYPE input = "1", the U.S. standard is selected and when the TYPE input = "0", the C.I.T.T. standard is selected.
Tx Data	Transmission Data is the binary information input. Data entered for transmission is modulated using FSK techniques. When operating the U.S. standard (TYPE = 1), a logic 1 input level represents a Mark or when operating in the C.I.T.T. standard (TYPE = 0), a logic 1 input level represents a Mark.
Tx Car	Transmit Carrier is a digitally-synthesized sine wave derived from a 1.0 MHz oscillator reference. Frequency characteristics are:

United States Standard   **TYPE = 1**
Transmit Frequency   **ECHO = 0**

Mode	Tx Data	Tx Car
Originate 1	Mark 1	1270 Hz
Originate 1	Space 0	1070 Hz
Answer 0	Mark 1	2225 Hz
Answer 0	Space 0	2025 Hz

C.C.I.T.T. Standard   **TYPE = 0**
Transmit Frequency   **ECHO = 0**

Channel 1	Mark 1	980 Hz
No. 1 1	Space 0	1180 Hz
Channel 0	Mark 1	1650 Hz
No. 2 0	Space 0	1850 Hz

Echo Suppressor   **TYPE = 0**
Disable Tone   **ECHO = 1**

Chan. No. 2 0	1	2100 Hz

Symbol	Function
Tx Enable	Transmit carrier output is enabled when the Tx Enable input = 1. No output tone can be transmitted when Tx enable = 0.
MODE	Mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation. When Mode = 1, the U.S. originate mode is selected (Type input = 1) or the C.C.I.T.T. channel No. 1 (Type = 0). When Mode = 0, the U.S. answer mode is selected (Type = 1) or the C.C.I.T.T. channel No. 2 (Type input = 0).
ECHO	When Echo input = 1 (Type = 0, Mode = 0, Tx Data = 1) the demodulator will transmit a 2100 Hz tone for the disabling line echo suppressors. During normal data transmission, this input should be low = 0.
Rx Data	Receive Data output is the digital data resulting from demodulating the Receive Carrier.
Rx Car	Receive Carrier is the FSK input to the demodulation. This input must have either CMOS or TTL compatible logic level input (see TTL pull up disable) at a duty cycle of 50% + −4%, that is a square wave resulting from a signal limiter.
Rx Rate	The demodulator has been optimized for signal to nose performance at 200, 300, and 600 bps. The Receive Carrier must change frequency for more than half of the selected data rate period before the Receive Data output will change.

Data Rate	Rx Rate	Type
0-200 bps	1	0
0-300 bps	1	1
0-600 bps	0	1

Symbol	Function
SELF TEST	When a high level (ST = 1) is placed on this input, the demodulator is switched to the modulator frequency.
Reset	This input is provided to decrease the test time of the chip. In normal operation, this input may be used to disable the demodulator (Reset = 1) — otherwise, it should be tied low (0).
Osc in, Osc out	A 1.0 MHz crystal is required to utilize the on-chip oscillator. A 1.0 MHz square wave clock can also be applied to the Osc in input to satisfy the clock requirement. When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be < 9 PF at the crystal input.
TTLD	To improve TTL interface compatibility, all inputs to the MODEM have controllable P-channel devices which act as pull-up registers when TTLD input is low (0). When the input is taken high (1), the pull up is disabled, thus reducing power dissipation when interfacing with CMOS.
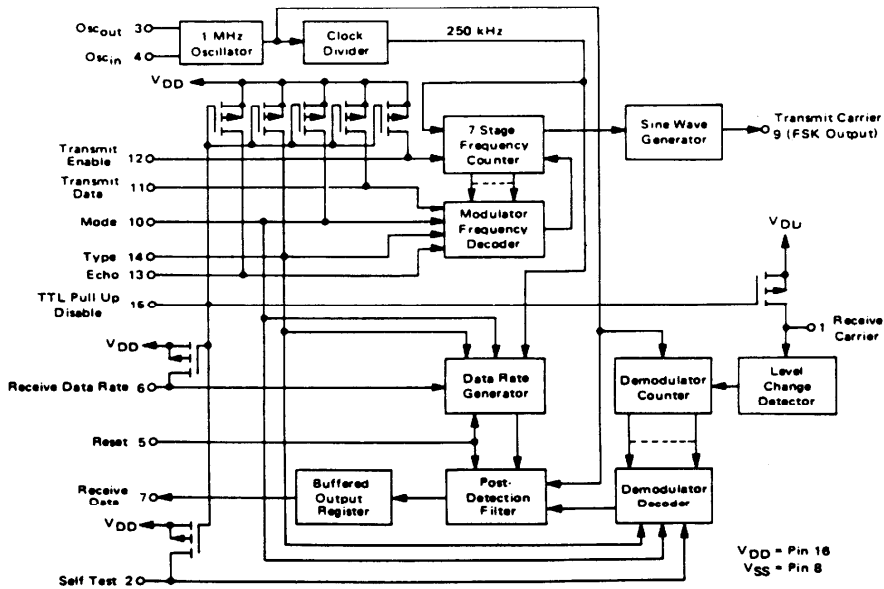
Figure 10-20. MC14412 System Block Diagram
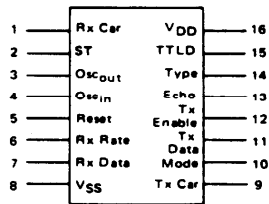
Figure 10-21. MC14412 Pin Layout
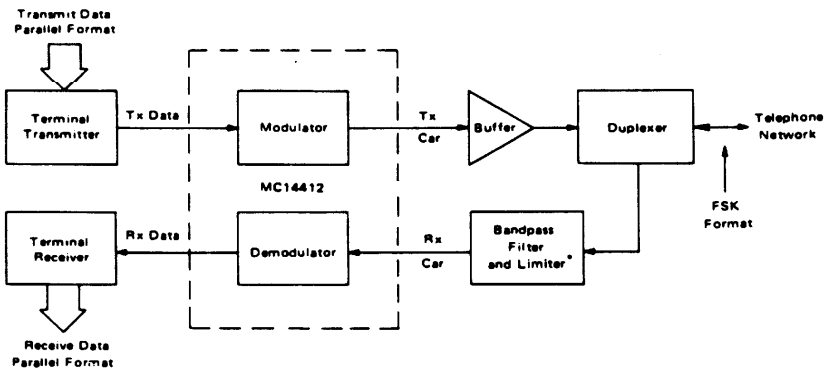
Figure 10-22. MC14412 Application Diagram

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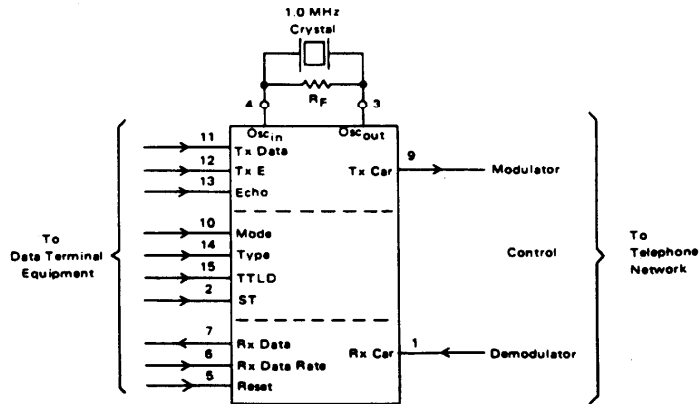
Figure 10-23. MC14412 Input/Output Signals

TC5518BF-25 (RAM)

TC5518BF-25 is a 16384-bit high-speed and low-power, fully static Random Access Memory organized as 2048 words by 8 bits. This IC has two chip enable inputs, CE_1 and CE_2, which are used for device selection and can achieve the minimum standby current mode for battery back up.

(TOP VIEW)
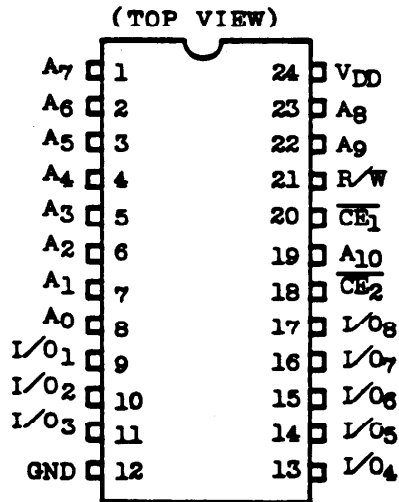
Figure 10-24. TC5518BF-25 Pin Layout

Pin Name	Description
$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
CE_1, CE_2	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
GND	Ground

Table 10-6. TC5518BF-25 Pin Assignment

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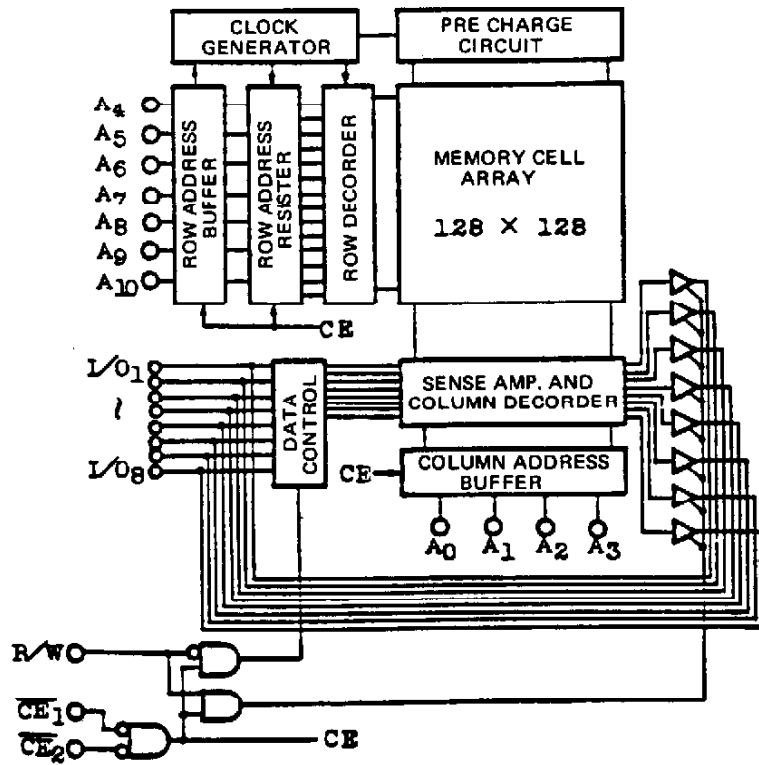
Figure 10-25. TC5518BF-25 Block Diagram
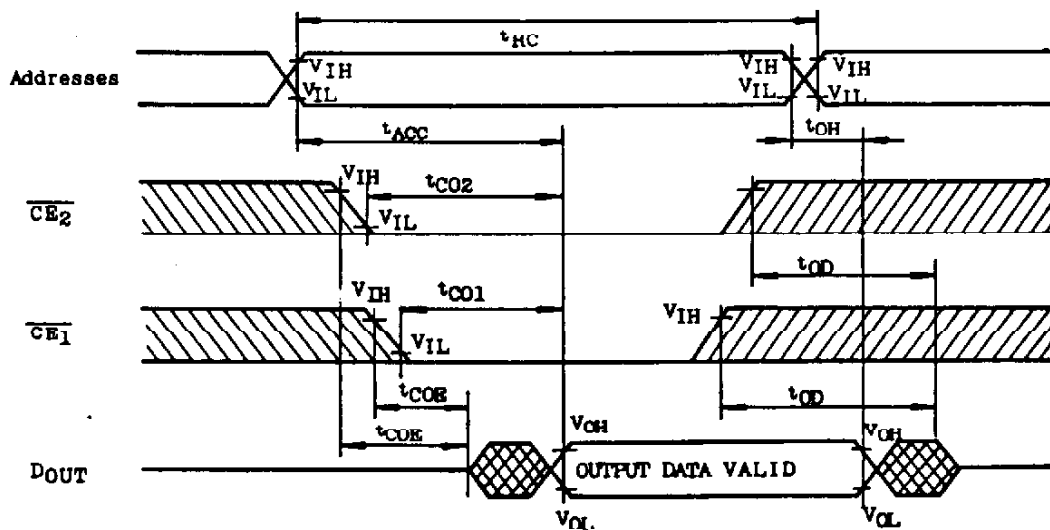
Figure 10-26. TC5518BF-25 Read Timing Diagram

Write Cycle 1.

Write Cycle 2.

⬛⬛⬛ : UNKNOWN
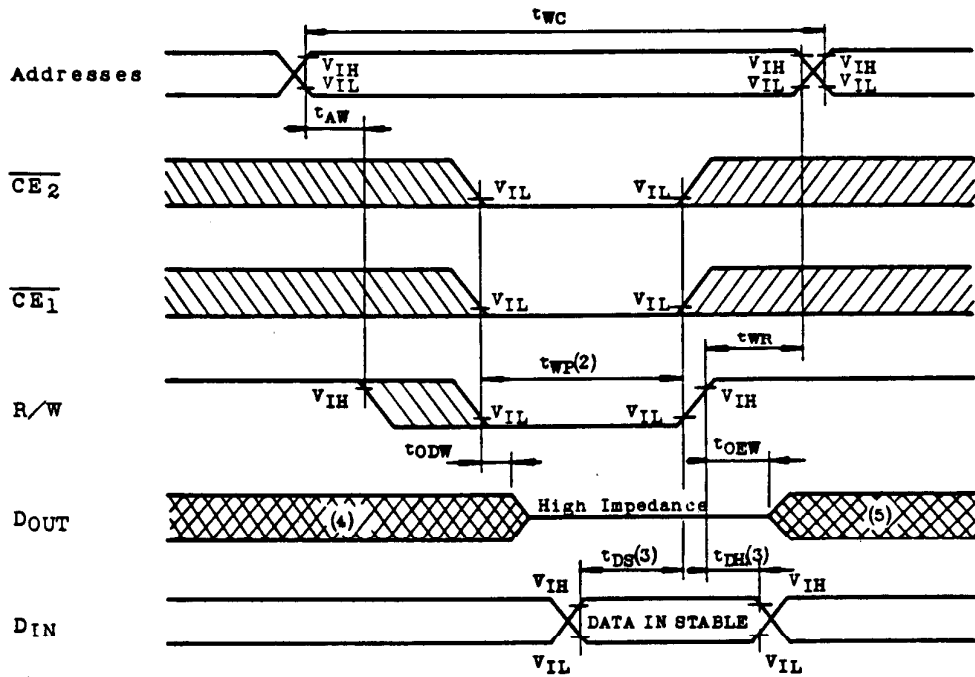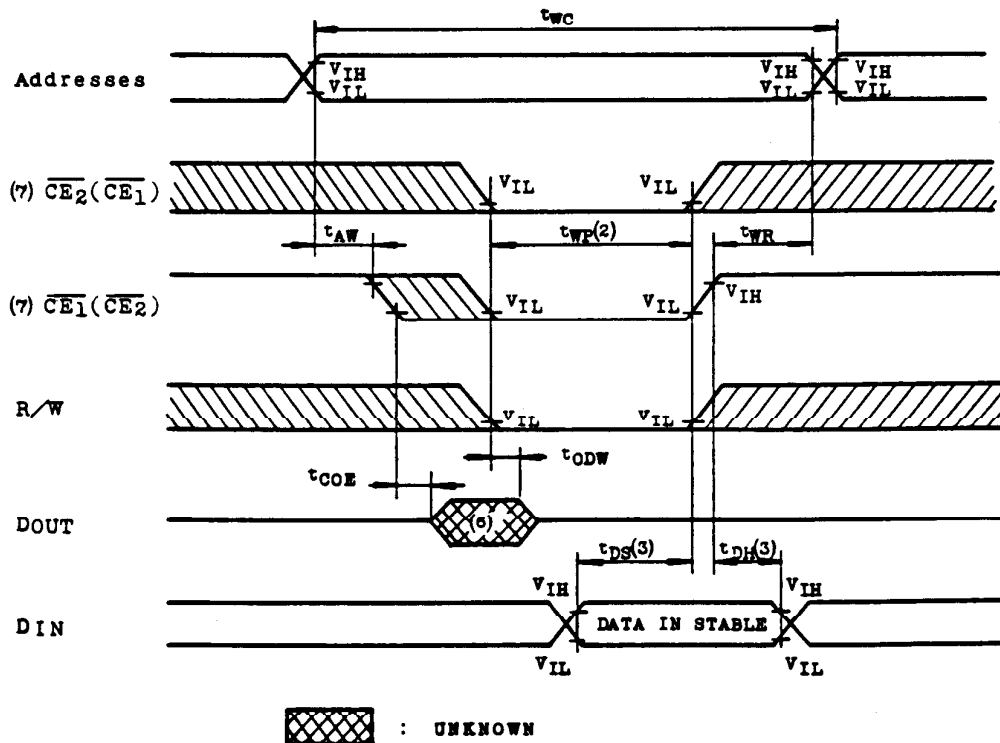
Figure 10-27. TC5518BF-25 Write Timing Diagram

LH-535618 (ROM)

The LH-535618 is a static mask Read Only Memory organized as 32768 words by 8 bits, fabricated with silicon-gate CMOS process.
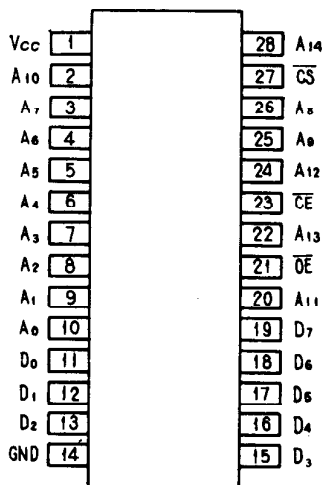
Figure 10-28. LH-535618 Pin Layout

Pin Name	Description
$A_0 \sim A_{14}$	Address Inputs
CS	Chip Select Input
CE	Chip Enable Input
OE	Output Enable Input
$D_0 \sim D_7$	Data Outputs
V_{cc}	Power Supply

Table 10-7. LH-535618 Pin Assignment
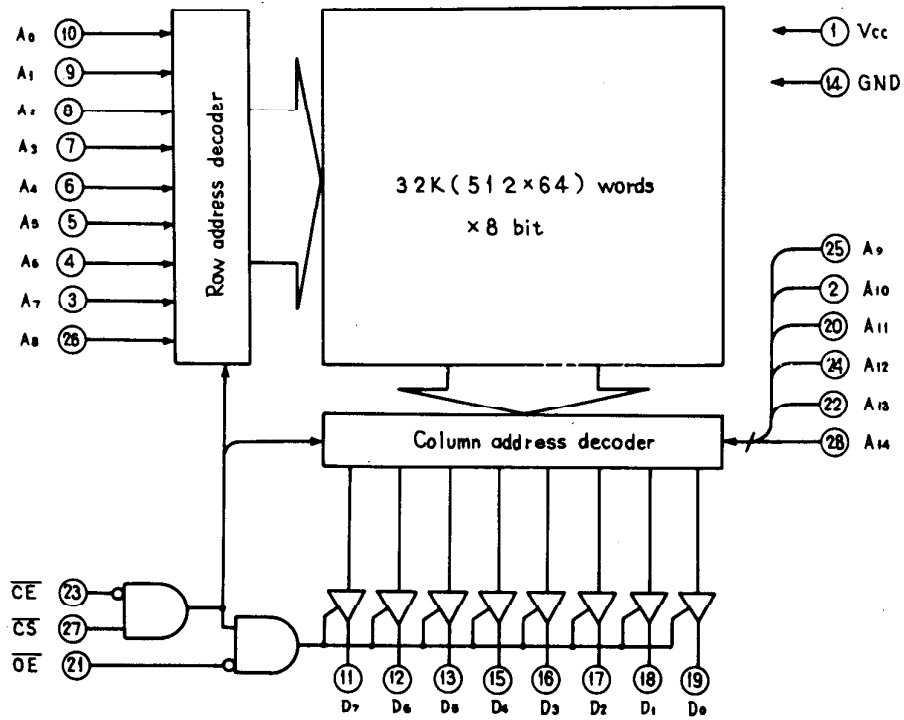
Figure 10-29. LH-535618 Block Diagram
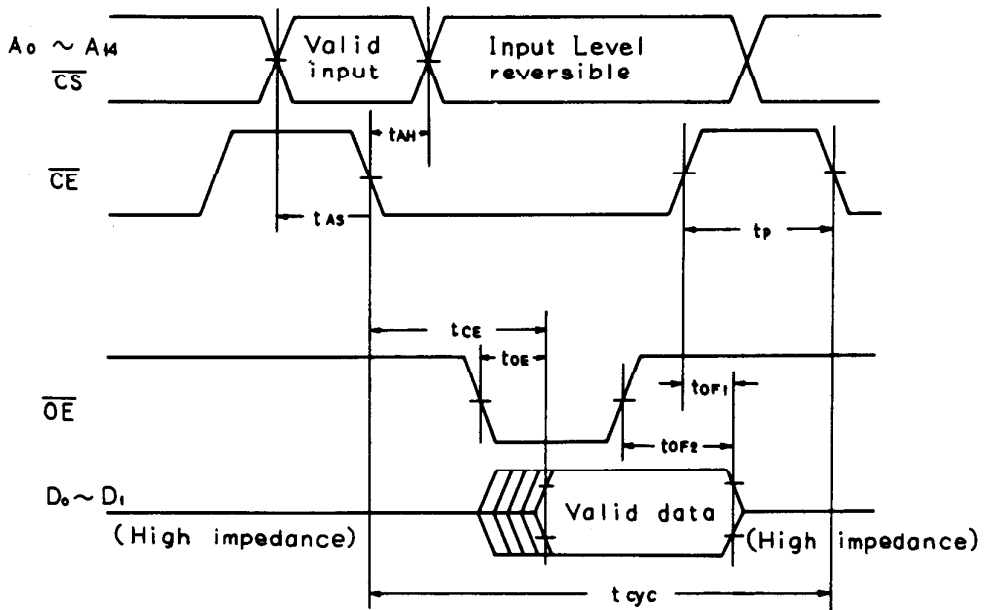
Figure 10-30. LH-535618 Timing Diagram

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